



THE HITCHHIKER'S GUIDE TO PCB DESIGN

Things You Wish You Knew Yesterday and Will Need to Know Tomorrow

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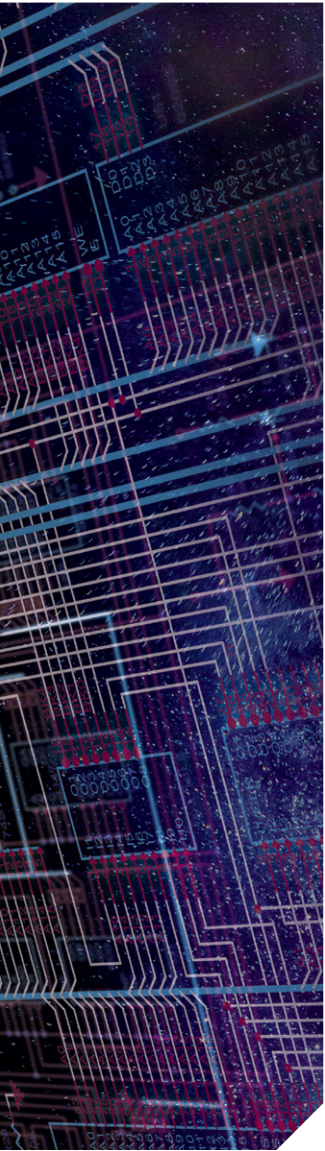


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Contributors

The Pros Who Have Been There and Done That



We understand the PCB design process is not done in total isolation. The success of any design project is dependent on the connections and contributions of the different stakeholders who contribute their insights throughout the process.

This guide was no different.

Throughout the creation of the guide, we here at EMA relied on the contributions from various industry experts. Their input was invaluable, and we want to take a moment to recognize and thank them for their hard work and time dedicated to making this project a success.

David Ruff

Principal Applications Engineer, XJTAG

David Ruff has over 15 years' experience within the electronics industry—most of which have been spent working on circuit board test.

His career began in the Military Aerospace industry doing digital circuit board and FPGA design before moving on to work for Cambridge Technology Group (CTG). Within CTG, he has worked on many different projects ranging from mixed signal ASIC design to high voltage/high density power supplies.

He currently works for the XJTAG part of CTG, focusing on circuit board test and working with customers who are designing and building everything from Bluetooth speakers to satellites in volumes of one-off to many tens of thousands a week.

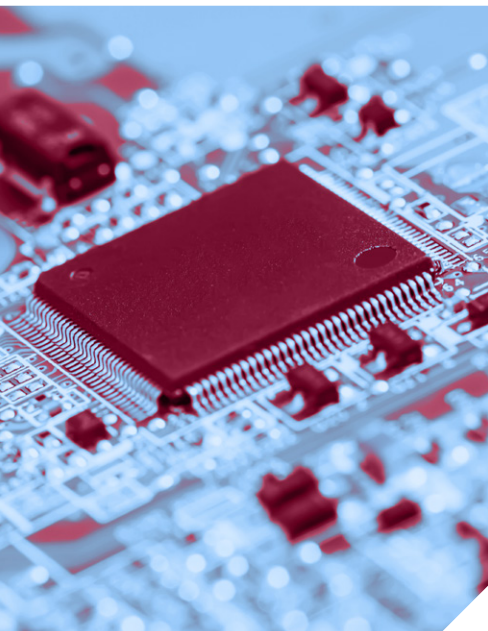
Jose (Joe) M. Bouza II

CEO, North Pointe Associates, Inc.

Entering the products development field as a youth, Joe Bouza currently has over 25 years of experience in the mechanical engineering field. He began his long career by attending college part time, taking many math and science courses and later focusing on advancing his career in the field of mechanics by learning many different aspects of mechanical engineering.

Joe started several consulting firms, the first being North Pointe Associates, incorporated in 1985, an engineering services company offering high-tech engineering consulting and product development services from concept to high volume production. Joe has kept North Pointe Associates, Inc. in a profit condition for many years. The ability to provide exceptional customer service to his clients is what keeps them coming back. Joe has been part owner of several other start-up companies such as Terra-Labs, LLC where he held the title of Vice President of Manufacturing, and Digital Adrenaline, LLC where he was a Principal, heading the mechanical engineering aspect of the company.

At various companies throughout his career, Joe has designed products for both the military and commercial industries. Products include but are not limited to a GC/MS mass spectrometer, moisture tension analyzer, cryptic alarm system with a battery backup, telecommunications equipment, and a medical dispensing product (Med-Aide) that keeps track of the quantity and time the medicine is administered.



Mike Brown

Principal PCB Design Consultant

Mike Brown has over twenty-eight years in the PCB Design industry. He began his career as a mechanical drafter and quickly moved through the ranks as a printed circuit designer, working for the likes of Commtek Inc (Long gone), GE, Lockheed-Martin, Martin Marietta, Kodak, CTA Space Systems, Orbital Science Corp. (serving Naval Research Labs – NRL & Goddard Space Flight Center) Ciena, Interconnect Design Solutions and Zentech Manufacturing.

The projects he has worked on included hardware designed for Aerospace, Military, and Telecom Sectors. In addition, the design types he has worked on include: power supplies (running as high as 120 amps on a single board), RF, High-Speed Digital with speeds @ 10G muxed up to 100G, Optical Drivers, Digital Cross-Connects, High Speed Switches, Transceivers, Muxceivers, Amplifiers, radio hand-sets, small explorer satellite sub-systems, ground support communications equipment, UAV's and wearable devices. His experience with PCB Technologies range from simple 2-layer boards on FR4, multi-layer HDI blind / buried vias on High Speed FR408 substrates such as Megtron-6, 0201 devices, Freescale 82xx processors, Stratix-V FPGA's, Compact-PCI, USB, DDR2 / DDR3 memory, up to 32-layer backplanes @ .250" thick using back-drilling.

Mike worked at Ciena for a period of sixteen years and during this time, he was awarded two patents. After his time there, he founded his own consulting group whose primary focus is on PCB Layout Development and Mechanical Engineering support.

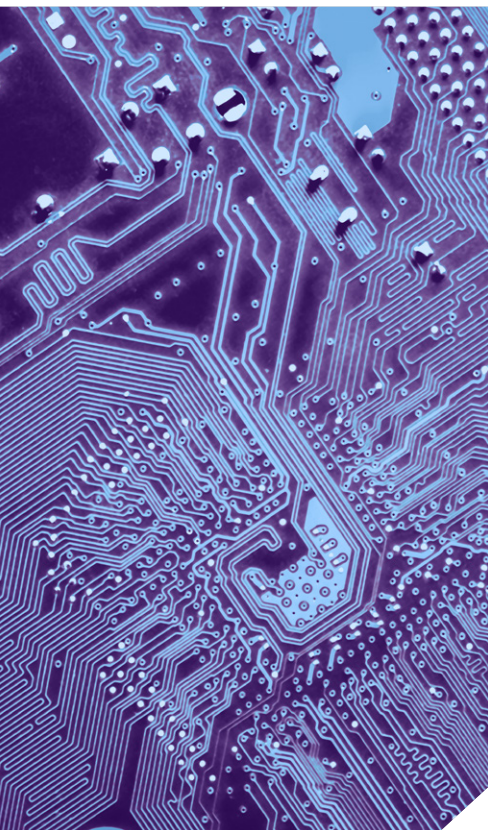
Patrick Davis

Senior Vice President, Rocket EMS

Patrick Davis is an industry expert with over 21 years' experience in the PCB design industry.

His experience has helped him to obtain a deep understanding of the Design, FAB, and Assembly process and their relationship to one another. His technical knowledge spans balancing ME, SI, Thermal, ID and EE requirements to execution of very large designs (1,000+ pins, 50+ layer), High voltage and power designs, DDR4, PCI-E Gen 3, 40GHz, HDI, Flex, rigid flex, and EDA tool management.

His Career began as a senior designer, launching his own business (which he operated for 10 years) before beginning his latest endeavour at Rocket EMS, where he is currently. Patrick prides himself on helping his clients resolve technology issues and create effective project management strategies.



Mark Thompson

Engineering Support/CID, Prototron Circuits Inc.

With a career spanning over 33 years, Mark Thompson has reviewed and worked with hundreds of thousands of data packages as well as thousands of customers' designers and engineers, helping them to create better data packages. During his long career, Mark has become one of the most trusted names in the industry when it comes to advising customers on how to productively work with printed circuit board vendors. Mark believes the PCB will be only as good as the data it takes to build it, and he has dedicated his career fulfilling this philosophy.

His popular column "The Bare Board Truth", Iconnect 007's most widely read column covers design, layout, and engineering practices as they relate to PCB fabrication.

In addition, he manages Prototron's own LinkedIn group, "PCB Bare Board Truth," a group devoted to Networking solutions to today's PCB fabrication issues.

Theodor Iacob

Power Systems Engineer

Theodor Iacob is an expert in electrical schematics and board layout with over 26 years' experience within the electronics industry. He is extremely knowledgeable in a wide range of systems and applications including: consumer electronics, high-speed analog, industrial, solar, and medical. He has experience in power design from mA to hundred amps, single-phase, multi-phase, buck, boost, and more.

He is an ambassador of schematic readability and believes while tools affect productivity, it is up to the designer to determine the quality of their schematics and layout. Currently, he is working as a Power Systems Engineer for one of the top technology companies in Silicon Valley.

Prologue

Why We Created This Guide

The industry is changing, there is no doubt about it. The job of an electronics engineer is evolving. Electronics Engineers are now tasked with additional PCB design tasks such as layout, component sourcing, DFM, collaborating with manufacturing, etc. While you may understand electronic theory, PCB design is an entirely different beast.

The goal of this book is to empower the new generation of 'PCB Design Engineers' to take on their additional role of PCB Designer knowing they have the foundation required to make sound design decisions or to ask the right questions when appropriate. The saying "you don't know what you don't know" is extremely relevant in this situation—how will you know what questions to ask about PCB design without some background in the PCB design process? Mistakes are inevitable and can be costly, but almost always preventable with the right knowledge base. Are there certain considerations you need to keep in mind throughout the design process? Where can you go for help when you need it? What PCB design best practices do you need to be mindful of? We answer these questions and more.

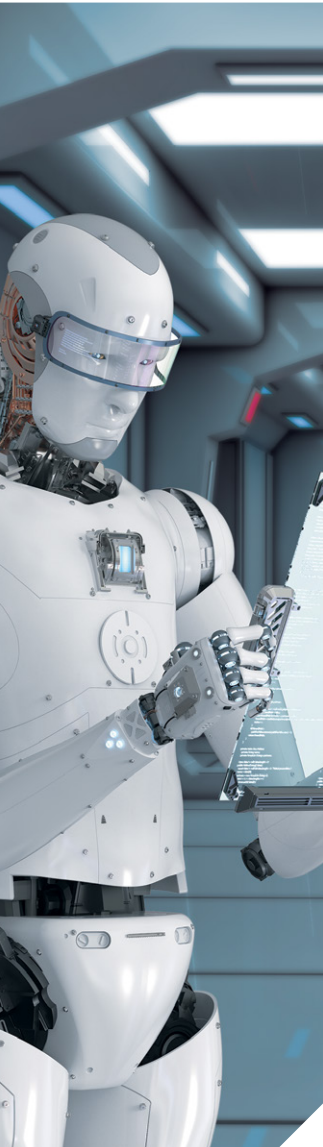
We didn't want to create just any other PCB design fundamentals book, so we decided to have fun with what could be a dry topic and take a more "fantastical," tongue-and-cheek approach. This book is intended to be a guide. Not the end of the story, but the beginning. Chapter's 1-3 introduce you to Ian, a new electronics engineer turned PCB designer. You will follow his journey into PCB design and the common mistakes he has made along the way (some of which may seem familiar to you). While his story is complete fiction, the truth is, Ian's story is one that is all too real.

If you aren't a "story person," feel free to skip Ian's story and start with any chapter that may be of interest. While we believe the sequence the book is written is the most logical way to present the process, there is no reason why you couldn't move from chapter-to-chapter in any order you please. Unlike the original Hitchhikers Guide to the Galaxy, you won't get lost in the story if you skip around. However, like the original we hope you will enjoy the journey, learn something useful, and possibly have a little fun.

Get your towel ready...

Chapter 1

A New Design Gig



Ian opened his email and was pleased to find an offer to work as an electronics engineer developing PCB designs for E-Z Galaxy. E-Z Galaxy is an established product development company not far from Zagon University, where Ian had just graduated with a degree in Electrical Engineering.

On his first day, Ian was shown to his new office by a robot named “Otto,” who performed all the company orientation and HR routines automatically. Upon Ian’s arrival, Otto performed a full-image body scan on Ian and prompted him to state his name and title aloud.

“Ian, engineer... Er, uh, PCB designer,” Ian responded.

“Match. Welcome to E-Z Galaxy where experience moves aside for automation,” Otto said in a rather monotone electronic voice. “Please follow me to your office”.

Otto rolled past Ian and led him along a hallway of engineering office doors to a “de-escalator,” which carried them down a single floor to a solid oak office door. On it hung a sign that read: Designer of Printed Circuits. Behind it was a basement office filled with old furniture and drafting equipment from the sixties era. A drafting table, some T-squares, a light table, and ink pens were neatly positioned throughout the room. Ian noticed a new desktop computer set up on an old oak desk.

Otto rolled toward Ian and said, “Ian, you have been hired to replace Robert Gridmaster. He was automatically retired after accumulating 4,200 hours of vacation time during his long tenure with the company.”

“How long did Mr. Gridmaster work here as a PCB designer?” Ian asked Otto.

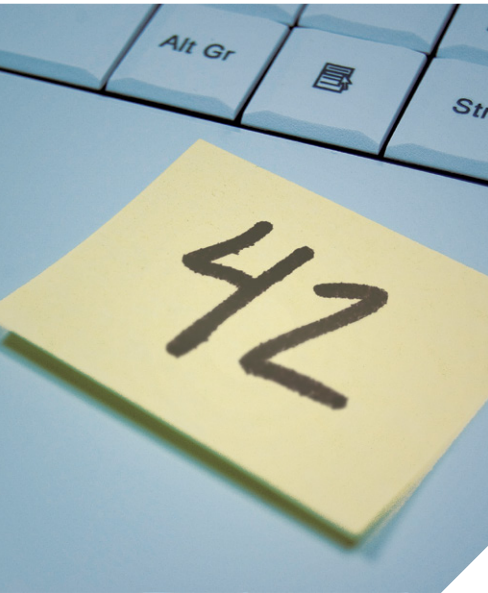
“42 years,” Otto said.

“This guy must have reached PCB design guru status.” Ian uttered under his breath. “It must have been difficult to let him go.”

“May your lack of experience, coupled with our culture of automation serve E-Z Galaxy well,” Otto responded. Then he rolled out the door.

After a few more days, Ian met some co-workers who had heard Ian was the new PCB designer replacing Robert Gridmaster or “Old Bob” as they called him. When Ian asked about Old Bob’s office and specifically, the process he used to design PCBs for the company, nobody could tell him much. They just went on about how they were going to miss him because he made PCB design look so easy. It wasn’t long before Ian began to discern his co-workers didn’t really have a large depth of knowledge regarding Old Bob and his role as a PCB designer.

The schematic software, with its automated presets, seemed to pull Ian along throughout the night and into the next day.



Ian began to think a lot about Old Bob, how did he always make PCB design look easy? He couldn't let go of the idea that Old Bob must have gained a lot of experience while working at E-Z Galaxy. He postulated Old Bob never wrote down his workflow and process for others to consider because it may have exposed any complexities associated with PCB design. Without a process and a workflow, a wave of panic coursed through Ian's head.

Ian was beginning to see before he had even started his new career as a PCB designer the company culture had taken his role for granted, considered it automated, and therefore deemed it easy. Ian was expected to know things about PCB design he was never taught in university, and had no one to turn to with questions. It was then Ian began to ponder to himself, with Old Bob gone, who will mentor me in PCB design as I start my career here at E-Z Galaxy?

Friday afternoon Ian received his first PCB project: The whiz-bit module. It was to be an "easy one" according to the project manager who was expecting "Old Bob-like" results by the following Monday. Ian didn't know where to begin. He turned on his new computer and noticed a post-it note on the desktop under the keyboard. Scribbled on the note was the number 42. Ian typed 42 on the keyboard and a template for a schematic immediately appeared on the screen. "Wow, that was easy," Ian whispered out loud. "There might be something to this automation thing after all".

Ian began capturing the schematic using techniques he remembered from the three-day PCB design course offered at Zagon University. The software defaults were pre-set and the schematic seemed to capture itself with each click of the mouse. Though it seemed to have taken only an hour to capture the schematic, when Ian looked at the clock he soon realized it was six AM! The schematic software, with

its automated presets, seemed to pull Ian along throughout the night and into the next day. It was as if Ian had not led the design software, but the software had led him. He could not remember the last time he'd blinked; he rubbed his eyes and wondered how schematic capture could be so automated, so easy.

Ian knew in order to finish the PCB layout he would need to start immediately. With the same automated ease he had with the schematic, Ian initiated a design template to begin the PCB layout. He created his own board outline and it wasn't long before he discovered an automatic parts generator. With a click of the mouse, a drop-down menu appeared for automatic parts placement, via fan-out, routing, design rule checking, and data output. PCB design really did seem easy at E-Z Galaxy using this automatic layout tool.

As he clicked the automated design routines and watched how quickly they ran, Ian felt the urge to rub his eyes again. He focused on his computer screen clock to realize he had again pulled an all-nighter and Monday morning had arrived. He realized in order to keep things running like Old Bob, he would have to get the PCB data files out to the PCB supplier quickly. "Who builds these PC boards and how much do they cost?," he thought.



At seven AM, Ian's phone rang. His project manager called to ask how the layout was going. While Ian described how easy the project had seemed, the manager was just glad to hear he was able to complete the PCB layout as fast as Old Bob. During their conversation, the manager let on that Old Bob had always gotten boards ordered cheap and in the least amount of days possible.

"That is my plan exactly, sir!" Ian responded. Though he had no idea of where he is going to send the design files.

After hanging up the phone, Ian performed a Google search: Quickie-Cheapo PCB fabrication. Several PCB fabrication service companies appeared listed on his computer screen. He picked one based upon a customer rating of four-point-two stars and sent the PCB manufacturing data output to Etch-O-Matronic Circuits.

Ian was elated he was going to be able to get his designs fabricated easily by Etch-O-Matronic. It was easy to order PC boards for his new company. E-Z Galaxy furnished Ian with a credit card number and Ian sent along his PCB board data to Etch-O-Matronic with a request for the quickest turn-around time. After the online transaction, Ian received a nice message response:

THANK YOU FOR YOUR 24-HOUR, QUICK-TURN ORDER. DFM REVIEW IN PROCESS.

Ian thought about the acronym "DFM" for a moment. He had seen it before, but really didn't understand what it meant and brushed it aside from his thoughts. Just then, Ian received a phone call from the project manager asking for an update. Ian explained the design data had been sent to the fab shop and was scheduled to dock the next day.

"Excellent!" the manager replied.

Ian thought his manager sounded pleased with the way he leveraged automation to make up for his lack of PCB layout experience. However, (though Ian was not aware) his manager really felt more satisfied about how easy E-Z Galaxy's automated hiring system made it for him to replace Old Bob. His manager was amazed he didn't even have to think during the process. He just pushed the "hire" button on the HR system and shortly after the automated resume sorter had chosen Ian as a candidate for the new PCB designer position.

After speaking with his manager Ian realized he hadn't eaten all weekend. He searched the online company directory to order some food from the cafeteria. After a quick look at the menu, Ian groaned, only cake was listed.

"Simple, like everything here—just a piece of cake," Ian whispered. Then he put his head down onto his desk and fell asleep.



Things to consider when starting a new job as a PCB designer:

- ☐ Investigate the company culture to make sure it is compatible with your personality and work style.
- ☐ Does the company you wish to work for give you a sense that your job is valued and appreciated?
- ☐ What type of software tools are made available to the PCB designer? Are they sufficient?
- ☐ Does the company offer software training or will you be expected to hit the ground running?
- ☐ Will you work within an established design group or will you be a sole resource?
- ☐ Will you be allowed to build your professional network and participate in industry events?

Chapter 2

DFM, Not Just Another Acronym



Ian was startled awake by a loud, repetitive dinging sound coming from his computer. He clicked to see an email message from the prototype supplier.

YOUR JOB HAS BEEN PLACED ON HOLD FOR THE FOLLOWING REASON: TRACE WIDTH AND SPACING INCOMPATIBLE WITH OUR PROCESSING CAPABILITY. DIAL 42 TO SPEAK WITH A MANUFACTURING ENGINEER WHO CAN HELP.

Ian panicked. The layout software had made design seem so easy; why was this supplier having trouble? Ian dialed 42 and was connected to the Etch-O-Matronic Circuits' CAM department. He spoke with the CAM manager who turned out to be none other than Old Bob! He explained the nature of the disposition and helped Ian to see that just because his layout software allowed him to create one mil traces doesn't mean he should have. He went on to explain how to determine trace width with regards to performance and DFM.

Very grateful for having established a manufacturing contact who could help, Ian hung up the phone. He then retraced his design steps after opening the layout on his computer. He checked the pre-set design rules to see the program was set to route all the lines at one mil width. After half-an-hour or so, Ian found out fortunately all default route spacing settings were set to a value of 14 mils. Ian was relieved to see this. Since the spacing between the two one mil lines was set so wide, Old Bob's CAM department at Etch-O-Matronic could increase the traces automatically to a more manufacturable width of seven mils and still allow eight mils space between traces and continue with fabrication. Immediately, another email popped up:

YOUR JOB HAS BEEN PLACED ON HOLD FOR THE FOLLOWING REASON: DRILL SIZING IS INCOMPATIBLE WITH PAD DIAMETER LEAVING INSUFFICIENT ANNULAR RING. DIAL 42 TO SPEAK WITH A MANUFACTURING ENGINEER WHO CAN HELP.

Again, Ian dialed 42 and was connected to Old Bob who explained the design requirements and limitations of a plated through-hole and helped Ian adjust the design.

Throughout the day, this notification shtick happened over and over. Each time, Old Bob patiently described a manufacturing problem caught by Etch-O-Matronic's CAM department and each time he helped Ian correct the layout. Finally after getting dinged on just about every aspect of the design (which had been set to the software's automated default settings), the PCB design files passed all Etch-O-Matronic's design rule checks, and the PCB design was fabricated and automatically shipped to Ian's selection for an electronic manufacturing services provider: RoHaws, EMS.

Later, Ian received a tracking notification on his computer screen that the bare PCBs had just been delivered to RoHaws, EMS. Within the hour, Ian heard his computer ding repetitively, much like it did when he heard about manufacturing trouble from Etch-O-Matronic's CAM department. Ian received notifications the assembly job was on hold for numerous DFA reasons. Again, Ian was prompted to dial 42 to be connected with a manufacturing engineer who could help.

The quality of the assembly was out of Etch-O-Matronic Circuits' scope.



Ian dials 42 and was again connected with Old Bob. Wow, he really gets around for an old guy, Ian thought.

Old Bob disclosed to Ian there were some very serious design layout problems concerning this assembly which made the boards impossible to assemble. Ian pleaded with Old Bob to help him understand how a perfectly good PCB could pass through countless DFM rules at the board shop and then be considered scrap at the assembly shop.

Old Bob explained how, when finished, the bare PCB is considered a component. The quality of the assembly was out of Etch-O-Matronic Circuits' scope. It is the fabricator's job to create a quality component. The fabricator had no visibility regarding how the PCB would interface with all the other components.

Ian is dumbfounded. "How do you know the PCB cannot be assembled if you haven't even tried?" he asked.

"I think it's time you put on some virtual reality goggles," Old Bob said. Just as he finished talking, Otto entered the room carrying a strange looking headset and a lavishly soft, white cotton towel.

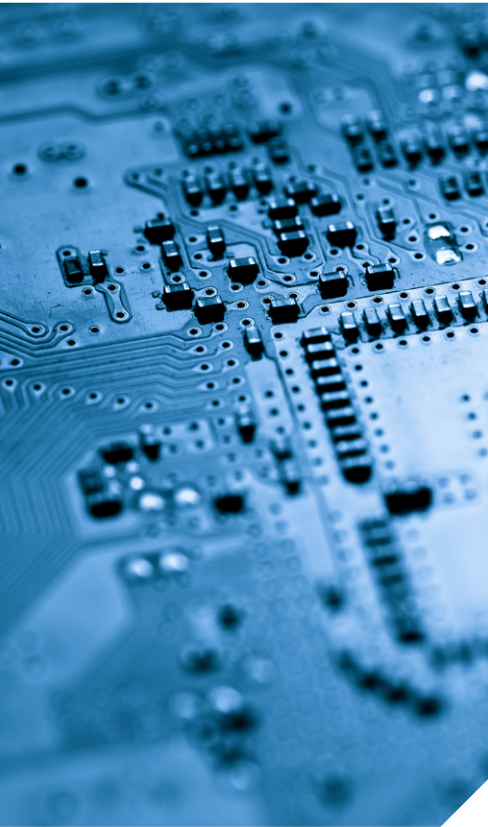
During his tenure at E-Z Galaxy, Old Bob explained how he'd developed a virtual reality DFM auditing app. This app allowed him to see the effects and virtual outcome of his design decisions on the various manufacturing processes before they ever actually hit the manufacturing floor. Ian asked what he should do with the goggles. "Well, put them on!" exclaimed Old Bob. "They'll let you see me here on the assembly floor and allow you to view a virtual play-by-play of your PCB on the assembly line."

"What is the towel for?" Ian asked.

"Oh, that?" responded Old Bob. "Whenever you review a design, virtually or otherwise, always keep a towel with you. It will come in handy."

Ian drew the straps of the goggles over his head and secured the viewport onto his face. The app immediately switched on giving Ian his first view of a man standing on the assembly floor of a vast warehouse-style building.

The inside of the building appeared to be very dark. Ian could barely see the man due to a haze covering the floor. The assembly machines came into view, but appeared smudged and burnt. He turned his head to search for Old Bob; the goggles seemed to be fogging up. Ian motioned for the robot to come close and hand him the towel. He gave the headset's viewing periphery a virtual swipe using the towel, and the same man—an older man in tattered clothes—came into view out from behind one of the machines. His hair was a steamy, curly mess and his face was blotched red as if it had been touched by sandpaper. The man was waving his arms frantically like he was trying to get Ian's attention—it was Old Bob! More smoke and now sparks began to shoot from one of the machines; Ian could see Old Bob mouthing the words, "Don't panic! Hit rewind... Hit rewind!"



Ian thrust his hand under the straps of the headset and tore VR goggles off his head. He frantically pressed a red button labeled: DON'T PANIC —JUST REWIND on the outer, lower-left corner of the goggles.

Ian shouted at the phone receiver which lay on the desk un-cradled.

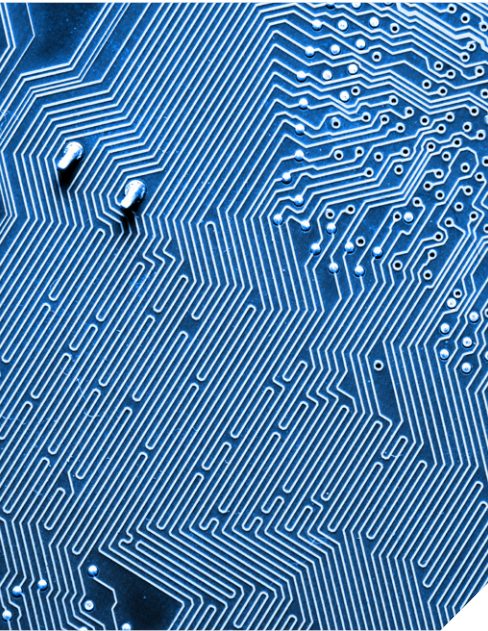
“Bob – are you still there?” Ian spoke loudly into the receiver. “I saw the floor, but it looked like World War III had just started. There was smoke and sparks and—!”

“Oooh my!” Old Bob chuckled. “You must have started the DFM review program in final results mode. The app kind of freaks out when there are too many DFM problems on a design.”

With a grandfather-like voice, Old Bob had a heart-to-heart with Ian. “We just did the best we could to drill the holes, etch, and plate copper to make it look like your PCB artwork. As I think you’re beginning to see, there’s a lot more to PCB design than just laying down tracks and making things look pretty,” Old Bob explained. “Now put those VR goggles back on and start the app in DFX mode. That mode will give you a virtual view of your PCB design from start to finish while stopping to show you all the basic Ws: Who, What, When, Where, Why, and How.”

Ian heard a click on the phone and realized Old Bob had hung up. Ian returned the black handset of the old phone to its cradle. Then, out of the corner of his eye, Ian caught a view of something attached to the robot’s vision units. It was another VR headset adapted uniquely for Otto the robot.

I guess he wants to come along and see how to fix my design, Ian thought to himself. Ian looked at Otto and said, “Here, hold my towel. It’s time to learn how to do things the right way.”



Ian's hard-learned lessons:

- ☐ Understand your layout tool settings. All of them.
- ☐ Do not trust default software settings to design your PCB. Understand how to optimize them.
- ☐ Learn which PCB and manufacturing standards are applicable to your project and follow them.
- ☐ Establish manufacturing contacts and mentors. Ask for advice and take advantage of free DFM checks before the design is sent for fabrication and assembly.
- ☐ Communication with all stakeholders is critical and is an important responsibility of the PCB designer.
- ☐ To design is to create, but successful PCB design is not done in a vacuum.
- ☐ A PCB design will only materialize successfully by a commitment from the designer to reach out and gather information from the PCB industry stakeholders which will all be contributing their part to manufacturing the design
- ☐ In the design and manufacturing industry, there are successes and failures every day. Success can be described as when a manufacturer can rely on accurate, sensible data to run the machines which produce the PCB which get the manufacturing jobs done as specified to meet the performance requirements of the PCB.
- ☐ Failure is the exact opposite of success. CAD software has enabled the world to sketch in PCB features and enter values for data which are far outside our present machine and process manufacturing capabilities.

Chapter 3

A Fresh Start: Introducing PCB Project Stakeholders



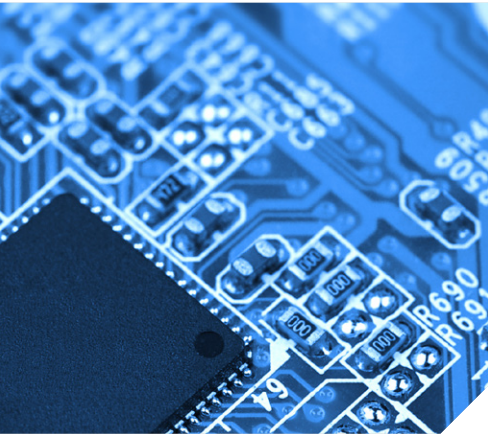
Ian readjusted the straps of the VR goggles and saw only darkness from behind the goggles until he heard a soft beep.

"Welcome Ian," Ian heard several voices speak unanimously.

Looking up, Ian could see seven other users seated around the table, including Old Bob and Otto the robot. Old Bob exclaimed to the users seated at the table, "This is the designer I've been telling you all about. His name is Ian and he is here to meet you and learn about your respective stakeholder requirements, so he can implement them into his next design."

Like Ian, it is critical to understand communication with all stakeholders is an essential and important responsibility of the PCB Designer. Successful PCB design is not done in a vacuum; the role of an Electrical Engineer has evolved. A PCB design will only materialize successfully by a commitment from the EE/PCB designer to reach out and gather information from the PCB industry stakeholders; all of whom will be contributing their part to manufacturing the design and ensuring its overall success.





The Program Manager

Before the engineering process of a project begins, the Program/Project Manager (PM) considers all the resources which will be required to complete the project. For example, in our story, one of the resources is Ian, the PCB designer. On a well-run project, the PM will ensure certain PCB designers (like Ian) are well-informed about important details regarding the PCB. The program manager, however, is not an expert in PCB layout and relies on the designer to query about any missing information in the design requirements at this essential phase. The two must define several important key factors upon which the layout will be based.

When conceptualizing the PCB project, a PM obtains specifications for how the PCB will be used. Performance is a key factor in selection of parts, materials, and processes for the design. In the early stages of product definition, a designer must seek to identify a performance class for the PCB from the PM to get the layout pointed in the right direction. If the PCB is specified for use in a toy, such as an inexpensive illuminated fidget spinner, the materials and processes selected for the PCB must be simple to keep costs low. If the PCB is destined for use in mission critical life support equipment, it will need to be designed with robust features and quality materials, regardless of cost. They must withstand advanced processing and handling to be service-ready when called upon to function. The program manager considers environmental requirements:

- Where will the PCB operate?
- Will it be exposed to moisture or heat?
- Will it need to perform in a vacuum working in a satellite out in space?
- What will need to be done with regards to part selection and layout to mitigate any hostile conditions?
- He also considers cost requirements: Is the PCB design a requirement for a school project, or intended for sale?
- How many PCBs will need to be manufactured?

All these questions are best addressed by the project manager during the initial phase of PCB design.

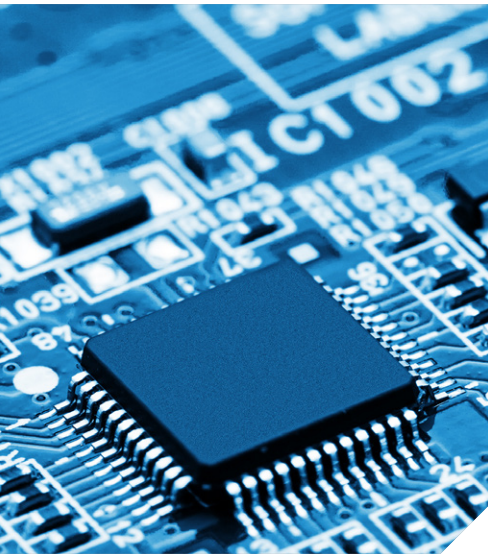
High level overview:

- Considers all resources required to complete a project
- Obtains specifications on how the PCB will be used
- Considers environmental and cost requirements

Works closely with:

- Electronics Engineer/ PCB Designer
- Mechanical Engineer
- PCB Fabrication Sales Engineer
- Assembly Manufacturing Engineer
- Test Engineer

**The industry
is now moving
towards a hybrid
role where the EE
and PCB designer
are one.**



The Electronics Engineer

Electronics Engineers (EEs) are well versed in circuit theory and the components which make circuits perform. They have spent their career devising creative ways to utilize electrical components in ways which would yield the greatest circuit performance at the lowest cost while providing for the requirements of many project stakeholders.

Since there is always so much in the way of design definition and specification required, there isn't much time to 'carve tracks' (although this is changing). Due to this reality, electronics engineers choose to collaborate on PCB design layouts. Traditionally, Electronics Engineers can provide PCB designers with either a rough draft or completed schematic diagram. However, the industry is now moving towards a hybrid role where the EE and PCB designer are one, the PCB design engineer, like our protagonist, Ian.

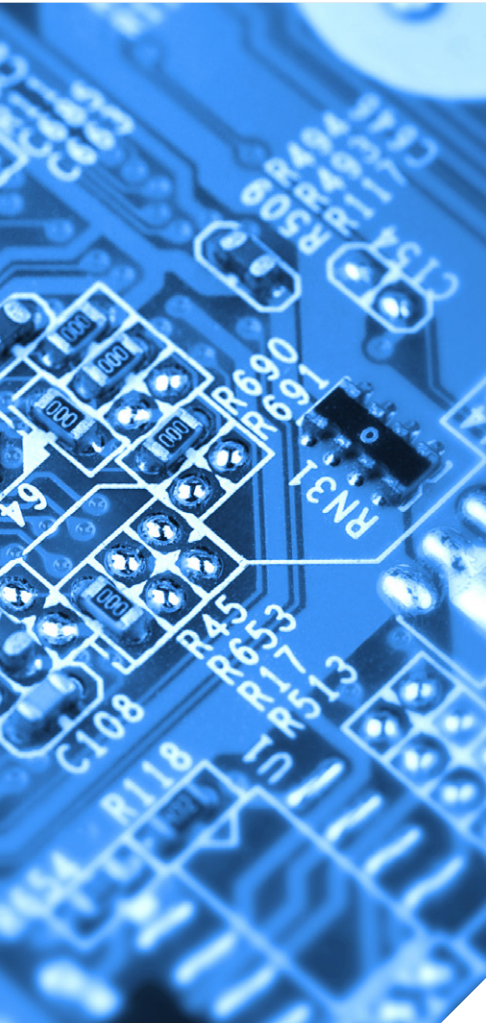
An experienced designer should already possess or know where to acquire the technical knowledge required for completing a design. The PCB designer should be able to give valuable feedback about the board layout density quickly, so adjustments to the parts list or part connectivity may be made.

High level overview:

- Responsible for design definition and specification on both the front and back-end of most projects
- Creates and provides the PCB designers with either a rough draft or completed schematic diagram of the design
- Provides valuable feedback with regard to board layout density

Works closely with:

- PCB Designer
- Project Manager
- Mechanical Engineer



The Mechanical Engineer

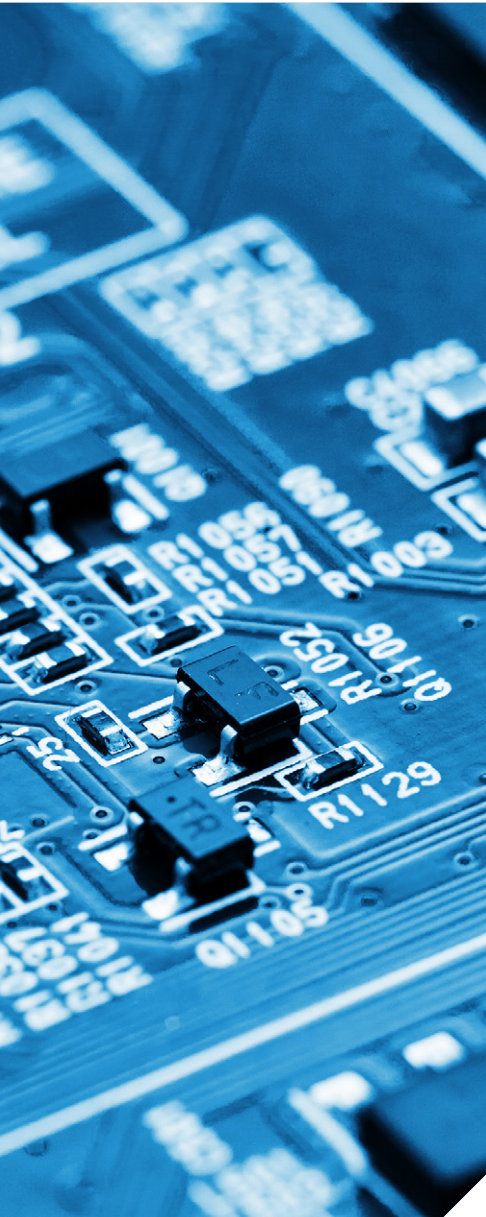
Mechanical Engineers (MEs) work hard for months creating solid model designs of the end product. The PM introduces the mechanical engineer to the industrial engineers (IEs) when the project begins (usually months before the PCB design is even a thought). The IEs create concept sketches and experimented with different sizes, shapes, and textures for the product. Once the best concept is chosen, the PM forwards the sketches to the ME so they can begin designing all the metal and plastic parts which would interface together to become the product. One of the parts the ME defines is the shape and size of the outline of the PCB, which is a critical component of the product. The ME touches base with EEs throughout the process to make sure the size and shape—the mechanical envelope—of the PCB works with all the electronic components the EE estimates will be required. Once the two stakeholders agree, the ME will freeze the PCB outline in the mechanical layout and begin designing other features around it, while the EE works to capture the schematic and may begin the PCB layout using the PCB outline as an important starting point.

High level overview:

- Designs all of the metal and plastic parts which would interface together to become a product
- Defines the shape and size of the PCB

Works closely with:

- PCB Designer/Electronics Engineer
- Project Manager



The PCB Fabrication Sales Engineer

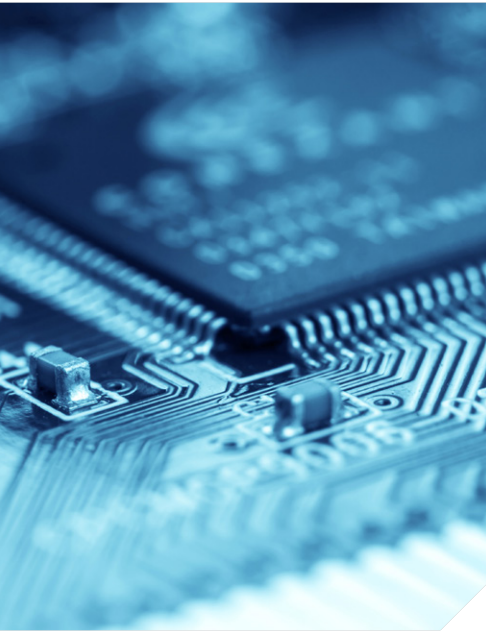
The PCB Fabrication Sales Engineer (FSE) works for the bare-board PCB supplier. They work diligently at their company to make sure the engineering customers' and the supplier management personnel's questions are answered by the appropriate technical people. If a PCB designer has a question about materials, hole sizing, or how to achieve a certain impedance requirement, the FSE connects the PCB designer with the right technical person to provide the answers. If a purchasing agent wants to order a quantity of PCBs to be delivered to the assembly house within five days, they coordinate with their company's quoting department in order to establish a cost and timeline. The bare-board supplier is responsible for creating the bare-board component from a given set of data within an agreed upon timeline and price. The success of the bare-board supplier is based upon the receipt of clear, manufacturable data. FSEs appreciate when customers ask questions they can find answers to before the PCB design data ever hits the shop floor.

High level overview:

- Works for the bare board PCB supplier
- Ensures engineering customers and the supplier management personnel's questions are answered by the appropriate people within the PCB supplier organization
- Responsible for creating the bare board component from a given set of data within an agreed upon time and agreed upon price
- Success is based upon receiving clear, manufacturable data

Works closely with:

- PCB Designer/Electronics Engineer
- Purchasing agent



The Assembly Manufacturing Engineer

The Assembly Manufacturing Engineer (AME) is a master at figuring out how to put a lot of parts together in the fastest way possible—with the highest yield at the lowest cost—by using the best machines and processes. They know when a PCB has been designed well; it means things will go well for their machines.

AMEs believe every good project begins with a well-scrubbed and validated parts list or bill of material (BOM). Most of the assembly process relies on auditing these listed parts for pricing, availability and lead time. In parallel, the parts are also verified against the layout for package configuration, form, and fit.

AMEs base their BOM checks and comparisons on intelligent manufacturing data in ODB format. Once all the Design For Assembly (DFA) checks are complete and the PCB assembly project begins, all of the parts are kitted to be assembled onto the bare PCB, which is also considered an electronic component.

While a PCB layout is designed only once, it sometimes spawns thousands of PCBs from the bare board supplier. Like PCB bare-board suppliers, AMEs love it when designers ask them about important things to consider for assembly before starting a layout.

High level overview:

- Responsible for putting parts together in the fastest way possible with the highest possible yield at the lowest possible cost
- Audits validated parts lists/bill of materials
- Works closely with PCB designers/Electronics Engineers to ensure a hassle-free assembly process

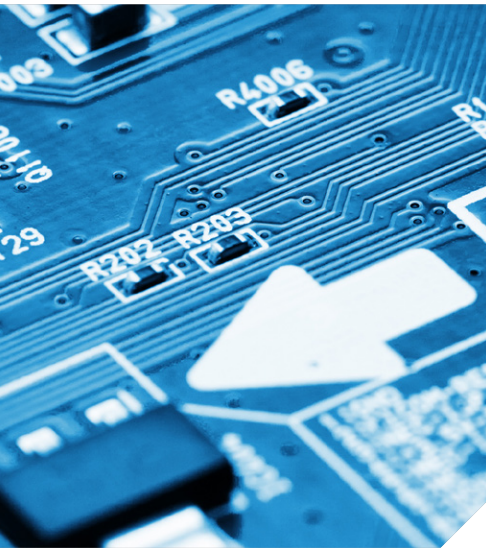
Works closely with:

- PCB Designer/Electronics Engineer
- Test Engineer

Pro-Tip From Patrick Davis

“Once there is a requirement for thousands of PCBs to be assembled from a single design, how the PCB was laid out—with regards to component size, placement, and spacing—determines if our machines will have an easy day or a difficult day. Don’t be afraid to go to your PCB assembly house to ask about any important items to consider before starting a PCB layout.”

**Both the TE
and the AME
know machines,
processes, and
people are not
perfect.**



The Test Engineer

The Test Engineer (TE) works with the EE to define the parts of a PCB assembly that will need to be tested. In high volume production, the ability to test specified features is critical to measuring success.

TEs also work with the AME to create automated test beds (or bed-of-nails test fixtures), which will be used to audit the success or failures of the AME's machinery and processes. Both the TE and the AME know machines, processes, and people are not perfect. There are thousands of things that can go wrong while manufacturing a PCB assembly. They know good design addresses the requirements for testing and auditing for manufacturing defects. Test engineers appreciate when a PCB design includes small test lands (etched copper "pads") they can probe with the pins on their test fixtures. Testing software is used with the equipment and once "probed" the test machines can catch most errors that might be introduced during the PCB assembly process.

High level overview:

- Defines parts of a PCB assembly that will need to be tested
- Creates automated test beds which will be used to audit the success or failures of machinery and processes

Works closely with:

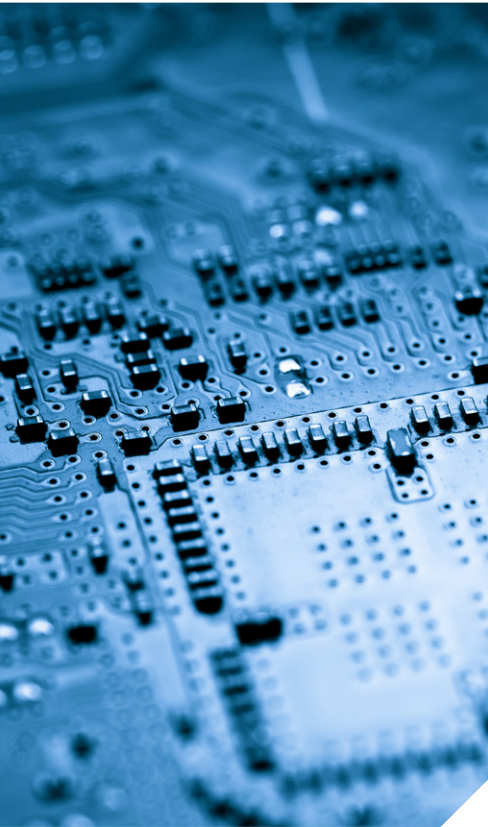
- PCB Designer/Electronics Engineer
- Project Manager
- Assembly Manufacturing Engineer

The Customer

The customer is the person you are designing the end-product for, be it internally or externally. They can be the person setting requirements or the end-user.

The customer's expectations are always high. All stakeholders know it is very important to work together so the customer's product will be made in the quickest way possible, with the highest quality, and for a reasonable price.

It is important to keep the customer in mind throughout the design process, so you can make design decisions that will support them. Items to keep in mind can be their level of technical expertise, where they will be using the product, etc. What may make sense to someone with technical experience may not be intuitive to a customer. Great engineers approach PCB design from an end user's point-of-view.



The PCB Designer/PCB Design Engineer

The PCB Designer's role as a stakeholder in a PCB design project is just as important as all other stakeholders. The chapters of this book are meant to illustrate this point by providing examples of what the PCB designer needs to bring to the project table and show why it is important and how it may be used by others. As we read of Ian's first experience at the project stakeholder table and how he became exposed to each stakeholder's process requirements and established workflows, we want to challenge all new designers to become familiar with the process of all the PCB project stakeholders. We want PCB designers to self-evaluate, asking themselves: What is my workflow? Do I even have a process?

Just as there are established workflows to guide the progress of a PCB panel through each of its manufacturing process steps, there is an established workflow for the PCB design process. To design a successful PCB, it is important to understand these design process steps by building stakeholder relationships. Keep in mind how every decision incorporated into the design will feed the success of the ensuing steps (and people involved) in the manufacturing process.

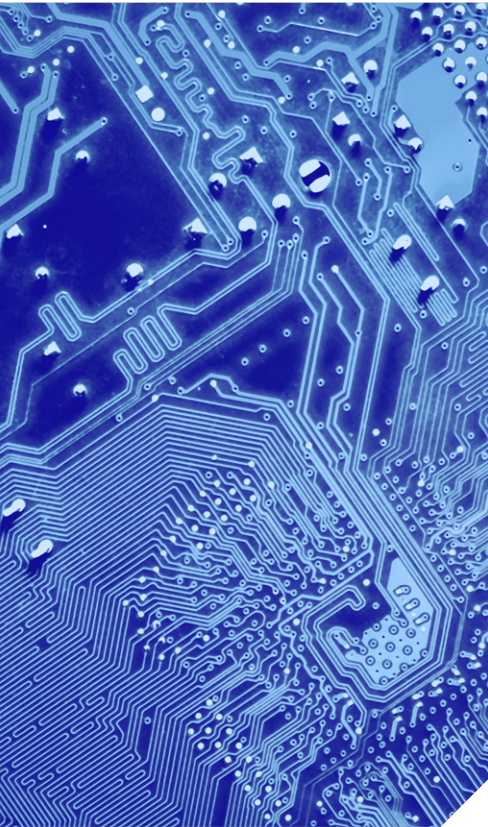
High level overview:

- Audits and organizes information and data from all project stakeholders to be included into the PCB layout
- Responsible for routing and creation of power and ground planes
- Responsible for all PCB fabrication data output and documentation
- Responsible for all PCB assembly data output and documentation

Works closely with:

- All stakeholders as required

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Contacting Stakeholders & Manufacturing Representatives

There cannot be enough emphasis placed on the value of developing a solid relationship with the supplier representatives and technical personnel who will be manufacturing your PCB before beginning the design process.

There is no better way to understand the materials and processes involved in manufacturing a PCB than to visit and tour the shop. Establishing a working relationship with EMS providers prior to starting a design will ensure the designer has a resource for solid manufacturing feedback when making important design decisions.

A great way to be introduced to the design and manufacturing community, its people, machinery, materials, process and software is to attend one of the many PCB design and manufacturing industry tradeshow held throughout the year. Electronics tradeshow are renowned for being interactive and informative gatherings where one can eat, sleep, and breathe all things PCB. Virtually all stakeholder representatives are always on hand to answer questions and to show off their materials, processes, and machinery. Company sales engineers often provide valuable samples which can be used for handy reference come design time. Strolling down an aisle of one of these shows can be like jumping right into a manufacturing workflow diagram for a PCB.

Popular PCB Trade Shows

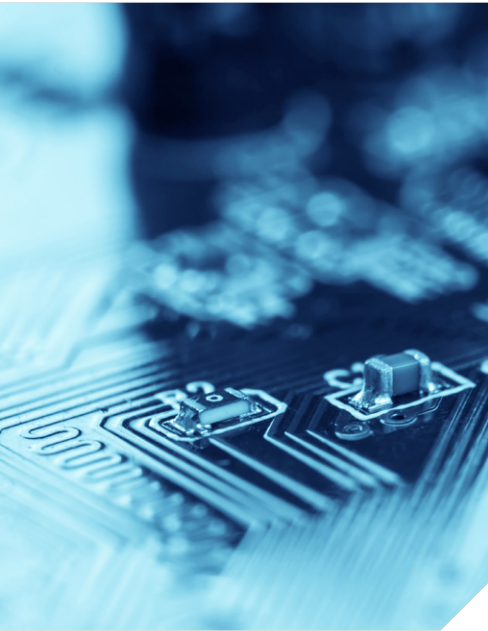
PCB WEST: www.pcbwest.com

IPC APEX: www.ipcapexexpo.org

DESIGNCON: www.designcon.com

SMTA: www.smta.org

Just as there are established workflows to guide the progress of a PCB panel through each of its manufacturing process steps, there is an established workflow for the PCB design process. To design a successful PCB, it is important to understand these design process steps by building stakeholder relationships. Keep in mind how every decision incorporated into the design will feed the success of the ensuing steps (and people involved) in the manufacturing process.

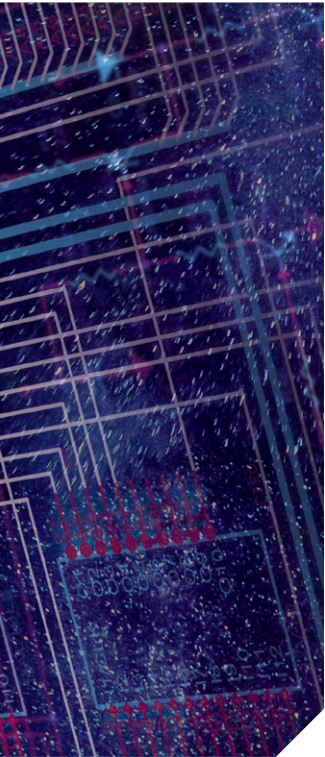


Some Items to Consider

- ☐ Examine all the constraints at the start of a design project before ever starting the layout.
- ☐ Acknowledge that what goes into a parts list will influence availability, size, shape, and performance.
- ☐ Determine what information will be included as the project is captured into schematic form.
- ☐ Evaluate PCB size and shape requirements—before the layout begins is the best time to get in touch with a good PCB fabrication supplier. What is the intended size and shape of the PCB?
- ☐ Raw materials for PCB fabrication are stocked in sheet form by the supplier. A designer needs to know if the available material can accommodate the PCB outline.
- ☐ Consider the parts placement and how a single design placement influences thousands of parts and operations.
- ☐ Recognize the need for testability. How the assemblies will be tested. Bed-of-nails or functional test, etc.
- ☐ Keep in mind the customer's desire for timely delivery, quality, and good price. All customer needs will be met in the end if all stakeholder needs are met before and during the project.
- ☐ Scrutinize your process. Things will go wrong. If you have a process in place, it will be easy to point to where a problem occurs and fix it so it doesn't happen again.

Chapter 4

Capturing the Schematic



In our story, Ian's schematic seemed to “capture itself” because he was using preset values of which he did not understand. However, before we delve into how to avoid a situation like what Ian had experienced, it is important to understand some key schematic design fundamentals, starting with what a schematic is and its main purpose.

A schematic is created by the electronic engineering stakeholder of a project. It serves the purpose of recording and communicating information about a PCB assembly's parts, connectivity, and functionality on the front-end of the creative process. The front-end of any electronics design project involves quick iteration and adjustment before any parts are purchased or copper tracks are laid down.

A schematic diagram uses simple, stick-figure symbols and lines to reflect actual electronic parts and circuit connectivity. Creating a schematic diagram is a way for an engineer to quickly document the elements of a complex circuit in a way that is easy to read and understand. A properly captured schematic helps the PCB design process by hierarchically organizing the electrical areas of the evolving PCB design.

A complex schematic drawing package, or design database, usually starts with a system-block diagram showing all the parts of the design on the first sheet. In a hierarchical schematic, users can click onto each of the system blocks on the cover sheet to be transported to a subsequent sheet of the schematic where the system block is expanded and drawn schematically. A completed schematic should look simple and basic to any viewing stakeholder such as a field service tech or test engineer. However, stakeholders such as those involved in design and layout leverage the vast amounts of data embedded within the ECAD schematic to complete the design layout.

Throughout the years, engineers have been using some creative methods to capture schematics. Capture software has very few input requirements and can be used by anyone to make connections between almost anything. For instance, ECAD tools today are so easy to use even a surfer with no electrical knowledge could create a schematic symbol for a beach hut, a surf shop, a surfboard, and a wave and tie them together with connections to show other surfers what he would be doing throughout the day:



Examining this simple schematic, it is easy to see the surfer is going to leave his hut, go to the surf shop, come out with a surfboard, and head for the ocean to surf a wave. Now, ask three different EEs to draw a schematic depicting a surfer's day and you will come up with some very different-looking symbols and schematics.

As you can imagine, each EE will have his or her own take on what the beach hut looks like: does it have a back door or a basement; is it solar powered or off grid? How an EE would depict a surf shop or surfboard schematic symbol is anyone's guess. When it comes to depicting a wave, well, let's just say EEs can be very knowledgeable about waves observed on an oscilloscope, but schematically depicting a wave viewed from a beach will again yield a wide variety of interpretations; leading to confusion amongst those trying to decipher these simple schematic drawings.

Common Schematic Symbols

Component *Reference Designator	Symbol
Diode (D*)	
Capacitor (C*)	
Inductor (L*)	
Resistor (R*)	
And Gate	
Nand Gate	
Or Gate	
Nor Gate	
Xor Gate	
Inverter (Not Gate)	
DC Voltage Source	
AC Voltage Source	
Ground	

The electronics industry foresaw this issue many years ago and as a result, organizations formed to standardize the way schematic symbols are depicted. ASME Y14.44-2008 and IEEE 315-1975 define how to reference and annotate components of electronic devices. The table to the left is a quick list of reference designators and their matching symbols. A complete list is on the IEEE association's website.

Successful schematic capture is basically the process of creating simple schematic symbols which contain basic nodal contacts. These symbols represent simple part configurations which are each documented on a page of the manufacturer's data sheet.

Individual component symbols are placed within the schematic's electronic database drawing sheets and connected with lines to form a schematic diagram. For organizational purposes, each symbol is assigned a unique alpha-numeric reference designation. Assignment of reference designator numbers can be performed manually or automatically. However, use caution in this area as some tools will allow duplications of symbol reference designators within the same schematic. After placement and connectivity of the schematic symbols are established, editing of the symbol and net information can take place to finalize the design intent.

It is important to recognize the goal of capturing the schematic for PCB design: to define or "capture" as much data as required to be imported into the layout database so it can be leveraged to create the physical aspects of the design. As previously mentioned, the schematic is a simplified, symbolic representation of what will materialize as a physical PCB assembly.

[Click to Enlarge](#)



Pro-Tip From Theodor Jacob

“I start by determining the goal when creating the schematic. At minimum, some engineers understand the [goal of the] schematic to get to a netlist—to essentially create the connectivity. Without the netlist you cannot move forward to do an actual layout. But if one thinks like that, one could create a netlist in a text editor directly, right? However, a netlist does not meet the requirement of ease of readability. So, secondarily I make sure the schematic I create will communicate my intent in a graphical form, such that it is readable, not just by me, but also by my peers.”

Just like Ian has discovered, there are many undesirable outcomes which can stem from naively using defaulted values and blindly launching software automation without understanding. If you were to replicate a simple schematic symbol hundreds of times in a schematic which contains incomplete or misunderstood data, the results would be catastrophic.

So ECAD suppliers have made schematic capture simple, right? Well yes, but it's not inherently simple. Over the years, in an attempt to help electronics designers address not-so-basic design issues by adding vast amounts of complex functionality, the ECAD industry has unintentionally made schematic capture rather complicated. It is now the responsibility of the EE to investigate these complexities, and understand them thoroughly, before even thinking of implementing them. As mentioned, a basic ECAD schematic library symbol performs the function of representing the connectivity of an electronic part within a circuit on the schematic. However, the explosion of ECAD tool functionality has required electronics designers to take on a

much more holistic view of the selected part. Information beyond pin assignment and connectivity can now be embedded into the part symbol. Electronic simulation models can be embedded for front-end signal integrity analysis. Attributes such as package type and even manufacturer's part number can be added. If that weren't enough, another click can get the EE into a cloud-based database, showing distributor's part numbers and availability. Still, more functionality can be added to the modern schematic symbol to access multiple PCB layout footprints which contain 3D representations of the part—a recent boon to the “mechatronics” movement which is quickly emerging.

As we can see, the simple building blocks of a schematic diagram are no longer simple due to advanced requirements for functionality. However, they remain the building blocks, so it is more important than ever to make certain every attribute entered into a fresh schematic symbol is accurate in every way.

Pro-Tip From Theodor Jacob

“If I have a good database with good library parts and all the necessary attributes added to the library parts, including: where to buy them, where they are in stock, the footprints, and any simulation information; that is absolutely helpful. But not all generic schematic tool libraries come with completed attributes such as these. There are, however, third party library sources which can provide them for a price if your company can afford to go that route. Regardless of whether a schematic symbol is purchased, or I build it myself, I like my schematics be able to be printed in .pdf form and have a user click onto the symbol to see it conveniently open a component data sheet.”

Before the layout ever starts, it is important all the performance criteria are clearly defined.



When creating schematic symbols, simplicity is key. There are not many rules regarding the creation of a symbol in a schematic unless they are pre-defined in an internal company design specification. For EEs working on a design team where there is a high probability created symbols may be used by others, and even for schematic symbol creators working on their own, it is prudent to consider that a symbol should have some form of consistency. It needs to be built on a nominal grid so it can be inserted into the schematic with solid connectivity. It must serve its purpose of identifying part and connectivity data. Symbol creators are free to replicate the part connectivity information in the symbol almost anyway they see fit, but for those without pre-existing company standards, there are a couple of basic guidelines which will help with consistency.

- For bi-directional discrete parts, consistently orient the symbol within the editor either horizontally, with pin one to the left, or vertically with pin one at the top. To build on consistency, assign the XOY0 origin of the symbol database at the origin of pin one. This will come in handy when quickly placing the part in the schematic.
- For uni-directional part symbols, follow the same guidelines as mentioned for bi-directional, but carefully consider information which may need to be added to the symbol to prevent the part from being installed backwards.

Schematically, a diode uses a graphic bar to designate the negative cathode end, but shall the cathode be assigned pin one or pin two? Surprisingly, data sheets from various manufacturers are not consistent on this. In most schematic symbol editors, the pin on the symbol may be designated “A” for anode and “K” or “C” for cathode to override this issue and better define functionality.

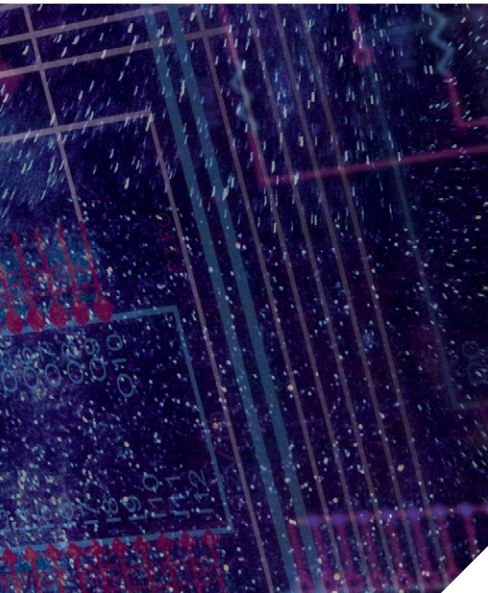
Component Selection

Before the layout ever starts, it is important all the performance criteria are clearly defined. Having a good understanding of the performance expectations of the Printed Circuit Board Assembly (PCBA) will help the design engineer to make the important trade-off decisions required at this phase of the design cycle.

Being able to address which performance class the PCBA will operate in should be considered first. Its performance has a lot to do with quality, and quality has a lot to do with cost. Will the PCBA be used on a toy that is mass produced? Cheap parts that perform for a limited time may be considered for the class 1 performance level. Is the PCBA expected to be used for a dedicated service application, such as an office printer or phone system? Parts for class 2 applications will need to be of higher quality and undergo minimal testing, so one would expect to pay more for these parts. Will the PCBA go into a product in which there will be dire consequences if it fails? Could someone get hurt? The Class 3 performance level requires all parts on the PCBA be of the highest quality and reliability to withstand stringent testing for survival in its intended environment. Parts for class 3 rated applications can be the most expensive.

Cost continues to play into a second consideration when selecting parts for a PCBA. The EE must be in touch with the mechanical stakeholder who has furnished some indication of size for the PCBA. Without consideration of size, the EE might decide to select a larger part or use multiple parts to save cost over a more tightly packaged, integrated solution. However, upon realizing the MCAD designer has only allotted a minimal amount of real estate for component placement, the EE may have no other choice than to sacrifice cost for packaging constraint considerations.

Smaller parts tend to pack together into designs requiring more density but see more defects and are more difficult to inspect.



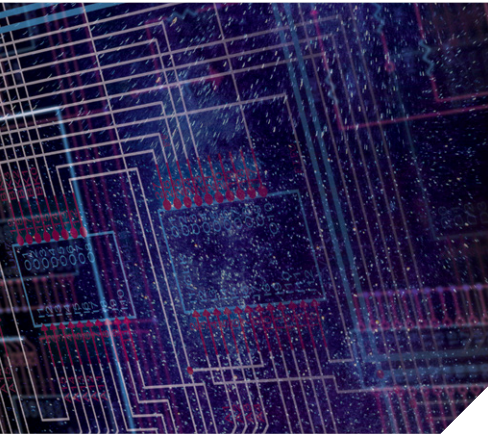
It is often interesting to observe a design team's dynamics about mechanical size vs. cost. For reasons unknown to the electronics stakeholders, the mechanical stakeholders tend to get the first crack at overall product sizing. They tend to design to impress by making surrounding enclosures as small as possible to reduce cost. Surprising dynamics come in to play when an EE stakeholder is forced to select more expensive parts to fit into the smaller enclosure, negating and even exceeding, any cost savings goals which the mechanical stakeholders were imagining. This will usually drive the stakeholders into an ebb-and-flow of negotiations to find just the right size-to-cost ratio. This is normal in the engineering phase and the quicker the team can come to a resolution, the more overall cost will be saved.

An additional consideration for component selection is packaging, which directly affects manufacturing costs. Electronic devices are packaged in many forms and supplied in various sizes. Component packaging technology—size, pin pitch, and soldering requirements—have a direct impact on manufacturing yield. Design scale must be considered by the EE when selecting parts. Larger parts tend to have fewer defects after running through the various manufacturing processes, but cannot fit into smaller scale designs. Smaller parts tend to pack together into designs requiring more density, but see more defects and are more difficult to inspect.

Another important consideration for component selection is the issue of availability. Just because the perfect part—one listing an acceptable performance rating, cost, and size—shows up on a supplier's data sheet is no reason for an EE to get excited. Whether or not the part can be procured at the right price, in volume, and is immediately available is a make-or-break issue. Availability is usually expressed in lead time – the time it will take the supplier to secure the parts and ship. If lead times are too great sometimes negotiating a higher price will help, but this will add cost and require some evaluation of cost-to-benefit ratio to determine if it will help or hurt the overall constraints of the PCBA project.

Setup and Definition

Now that we understand the factors that play into component selection, let's get into setting up our schematic. One of the first schematic setup steps the design engineer must perform when starting a new schematic diagram is to establish a grid value for the database. Modern schematic capture tools provide a variety of options, but how does one start? Imperial units or metric units? Which grid size? How shall the grid be represented—with dots or lines? These options are entirely up to user preference and should not have any effect on the schematic diagram—unless used improperly. Yes, so many options can confuse a new EE into making arguably the most common schematic capture mistake in the book—placing a symbol or a line off-grid and assuming it is contacting its electrical counterparts. The best advice for preventing this schematic faux-pas is self-discipline. Using a schematic tool, the EE must be extremely conscious of which grid setting is active while placing symbols and lines.



After setup of the placement grid, individual component symbols are placed within the schematic's drawing sheets and connected with lines to form individual circuits. Assignment of reference designator numbers are then addressed manually or automatically. However, caution must be used as some tools will allow duplications of symbol reference designators within the same schematic. For multi-sheet schematics it is very common to create a block diagram on the first sheet showing the various sections of the PCBA. A design hierarchy may be set up which will enable the user to drill down into any sheet section with ease.

Pro-Tip From Theodor Jacob

Regarding design grids, I think it's time to revise this concept because a .100-inch grid has no meaning schematically... When drawing a schematic, I concern myself with a page size. I use a page size that will allow me to decide how many wires I can draw from left to right and from bottom to top. I kind of choose the resolution of that page. I [believe we need to] shift the paradigm from thinking about grid points in metric or imperial units to how much detail can I fit on that page?

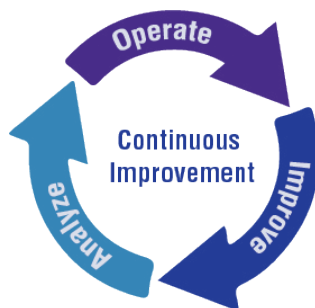
As mentioned earlier, the schematic is a simplified, symbolic representation of what will materialize into a PCBA. It is common for schematic symbols to be edited within the schematic (after placement) to define desired component packaging. Ultimately, the end goal is to define or "capture" as much data as required to be imported and leveraged into the layout database to create the physical aspects of the design. The same care taken when defining the raw schematic symbols needs to be taken in this process as well. Schematic entry

is base-level entry from which many downstream purchasing and manufacturing decisions will be made. It is imperative the data is entered accurately.

Haphazardly drawn schematic diagrams can serve the purpose of establishing connectivity and data output, but it is important the finished schematic diagram is understandable to all the project stakeholders. These are the people who will need to refer to it during the design review, layout, assembly, and test phases of the project.

Design readability can be a subjective issue regarding schematic capture. Therefore, it is best to consider existing industry standards (and even company guidelines) to aid in consistency of design and interpretation. It is important the schematic diagram flows and is organized in a way that is anticipated by the reader.

If you are new to creating schematic diagrams, reach out and shake hands with your project stakeholder counterparts to find out what they will be looking for. Will they be looking for any special notes in your schematic? How will some of the required performance characteristics be noted? Will current carrying capacity of lines be noted? What about impedance requirements? Will stakeholders be reading the schematic electronically or on paper? If the schematic will be printed, will the characters be readable based upon the size and scale of the output? If the schematic is printed as an electronic file (such as .pdf) can it be output in color with advanced capabilities such as being searchable? These are all questions to consider in the setup phase, before even starting the schematic. This ensures the schematic diagram will do its job to effectively communicate.



Finalizing the Schematic

The process of design engineering and continuous improvement is iterative. It's been said in every project there comes a time to do away with the EE and get on with production. This may be true, but until this time arrives, changes to the schematic are inevitable. In iterative design, it is common for a schematic to be subjected to a design review by an EE's peers (peer review) and then by the project stakeholders.

Ideally, once all feedback is received the schematic can be edited a final time and released for layout. However, this does not mean the schematic is formally released—the layout phase will invariably lead to some minor modifications to the schematic as the design moves from being abstract to physical. How these change requirements are managed is a combination of style and engineering protocol. Modern schematic capture tools work very well with layout tools to track and implement design changes. A schematic database, once edited, can quickly be compared to a PCB design layout and automatically update the layout to reflect the changes. A schematic and layout which has been automatically checked for part conformance and connectivity conformance are considered in synchronization.

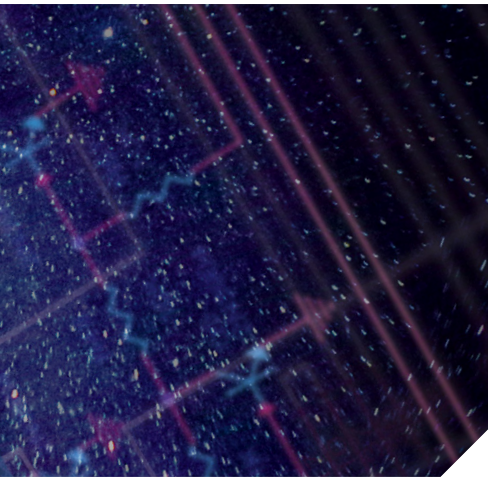
A schematic for a large PCB design can contain thousands of parts and hundreds of nets. With so much data, an EE can really begin to see the benefit of investing more time on the front end of a project to create standardized, accurate schematic symbols. Placing and connecting accurate, well-built symbols into the schematic can really pay off when it comes time to place, copy, and replicate circuits which will provide a clean netlist. This netlist output is used to drive the PCB layout software to pull all parts into the PCB database which will automatically be connected per the netlist connectivity strings.

Once the schematic is finalized, netlist output takes only seconds and is then imported into the layout just as quickly. Better still, most PCB layout tools which work together as a tool suite do not even need to go through exporting and importing of the parts list / netlist files. Modern schematic and layout ECAD tools work together well. They seamlessly reflect real-time connectivity between the two when viewed side-by-side as a cross-probable toolset.

Pro-Tip From Theodor Jacob

As far as the many schematic capture tool capabilities, I think that in the end, the tool that suits my interest best is the tool that helps my productivity and delivers results in the shortest time.

Schematic diagrams can range from very simple to very complex based on the design being captured.



A properly captured schematic helps the PCB design process by hierarchically organizing the electrical sections of the evolving PCB. However, care must be taken to ensure all the connectivity is established by running design checks after completion. It is very important to make certain all schematic nodes and wires not only appear connected, but are connected. A common error in schematic capture is to get caught slightly off grid while placing symbols and wires. The mismatch may be ever-so-slight and not visible, but enough to cause an open circuit. There is design rule checking for these type of errors, but errors regarding mapped footprints and pin numbering may be only caught by diving into the schematic windows. A properly captured schematic will only be successful if it projects the intended connectivity through to the PCB layout.

Schematic Outputs

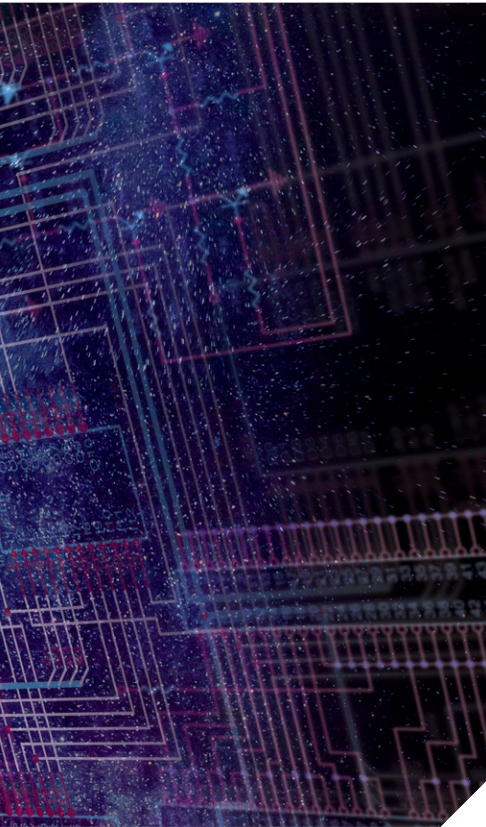
After checking, the BOM is sent to the purchasing stakeholder for quotation and the assembly stakeholder so parts can be checked for final availability and analyzed for processing capability. The data contained in the BOM can be uploaded to a company's MRP system for higher-level purchasing and inventory management. The BOM is usually output in the form of a text file or spreadsheet.

Another important output function of the schematic is a connectivity list or "netlist." The netlist in its simplest form can be viewed as a text file which is formatted to show all the circuit connectivity which will be imported into the PCB layout. The netlist format can be automatically exported and usually includes a header defining the format information followed by text strings describing the net names and their respective nodes. Netlists are useful to the fabrication and test stakeholders for verification purposes.

[Click to Enlarge](#)

Schematic diagrams can range from very simple to very complex based on the design being captured. However, the methodology used to capture the schematic can be kept simple by following industry standards, implementing consistency, common sense, and knowing what to watch out for.

[Click to Enlarge](#)

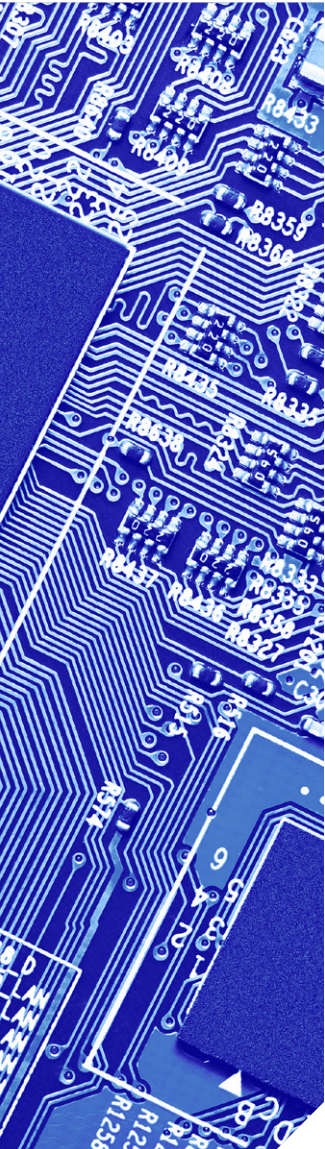


CHAPTER 4 SUMMARY/RECAP

- ☐ Follow industry standard guidelines for schematic capture: IPC-2612/IEEE STD 315.
- ☐ Consider the stakeholders who will be interpreting the schematic—communicate their needs.
- ☐ Start with a sound schematic library—create and modify new parts yourself using appropriate manufacturers' data sheets.
- ☐ Employ standard reference designations specified in the IEEE standards.
- ☐ For bi-directional discrete parts, consistently orient the symbol within the editor either horizontally, with pin one to the left, or vertically with pin one at the top. To build on consistency, assign the X0Y0 origin of the symbol database at the origin of pin one. This will come in handy when quickly placing the part in the schematic.
- ☐ For uni-directional part symbols, follow the same guidelines as mentioned for bi-directional, but carefully consider information which may need to be added to the symbol to prevent the part from being installed backwards. Schematically, diodes for instance may have their pins designated "A" for anode and "K" or "C" for cathode rather than being assigned a numeric value to more clearly define functionality.
- ☐ Check and double-check schematic symbols for accuracy.
- ☐ Use the symbol editor to assign the name and fill in the correct part information. Understand schematic symbols are the foundational building blocks of the entire PCB project: incorrect information in the symbol database can have catastrophic results.
- ☐ Cost is relevant to every process and material utilized in a PCBA. Carefully consider comprehensive processing costs of switching to an alternative component rather than its base price.
- ☐ Consider requirements of project stakeholders when determining schematic readability.
- ☐ Fully understand, and make good use of, the schematic capture tool's design check routines.

Chapter 5

PCB Layout: Setup and Placement



At this point in the project, Ian realized the power of having so much detailed information packed into the schematic, he believed anyone could perform the layout phase. However, what he failed to realize is a detailed schematic database is only the foundation for the PCB layout—not just anyone can perform a successful PCB layout. Layout must be performed by someone who understands industry standards for design and manufacturing as well as the depth of knowledge required for incorporating design for excellence. This individual is analytical enough to be able to sort through vast amounts of data, but creative and free-thinking enough to see many alternative ways to complete a design and have the intuition to choose the best one. A designer of PCBs is a person of renaissance.

Component Footprint Creation

Sometimes it is up to the PCB designer to create new component footprints for a design. A simple and straightforward process for footprint creation is best; it is also based on satisfying the stakeholder need to create perfect solder joints which could pass inspection of IPCs J-STD-001. If the component footprints are not correct and all assembly processes aren't taken into consideration, Assembly Manufacturing Engineers (AMEs) have a more difficult time soldering all the component pins to the PCB lands.

To yield a perfect solder joint there are three basic processes: paste screening for solder deposition, automated placing of components, and oven reflow of solder. The recommendations for land geometry are almost always provided by the component manufacturer, and they are best compared to the industry standard for creation of component land geometry, IPC-7351.

Setting up the Layout

Design automation can help to perform the first step in the layout process using personal layout templates. These templates are configured to contain a designer's favorite settings for common design environment items. They are often used for setting design units, layer colors, net colors, trace widths, and via sizing. They can be modified at any time during the layout to match the requirements of the design.

When setting up a new layout, design units can be set to metric or imperial units. Imperial units can be set to "inches," showing a decimal point in all values or "mils" (reflecting values in thousandths of an inch).

Convert Units of Measure

To Metric

Multiply by 25.4

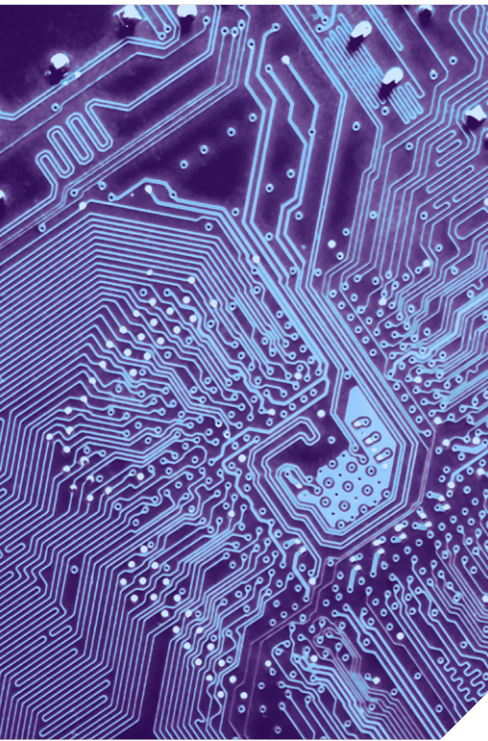
ex) 1.000 inch x 25.4 = 25.4mm

To Imperial

Divide by 25.4

ex) 1mm / 25.4 = .039 inch

To a new designer,
this state of confusion can appear
rather hopeless,
but this is where
the fun begins.



Defining the Mechanical Constraints

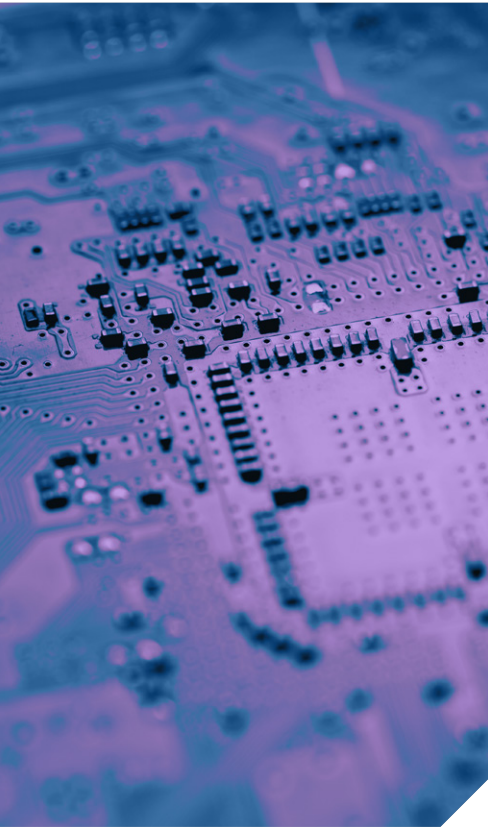
It is important to consider the complete definition of the PCB outline. There is more to a PCB outline than simply four lines to define a rectangle. In fact, PCB outlines are rarely defined as simple, rectangular shapes as PCB design continues to shrink electronics into the tightest useable spaces. Modern PCB outlines originating from advanced 3D packaging can contain complex curved edge requirements. Beyond mechanical consideration for the PCB outline is the defined thickness for the PCB. PCB thickness can range from very thick .200 [5.08] or more, down to .018 [0.46] or less. There are often mounting holes and slots, fixed component locations, and all the keep-out and keep-in definitions for the design. Sometimes, component height restrictions are defined in certain areas. Again, this type of constraint can either be imported or be defined manually after communicating with the mechanical engineer. One or more specific layers are reserved for the mechanical constraints. Additionally, intelligent auditing features can be added to the constraints definition. Most layout tools will allow the designer to define “rooms” or set up cross-hatched, keep-out areas which will alert the designer during design rules checking if there is a part within a keep-out zone. Once all the mechanical constraints are defined, the layout is ready for the next step.

Pro-Tip from Joe Bouza

“One of the things I see that is a big, big problem is that today’s ECAD/MCAD output files are not realistic enough. Sometimes components are only represented as blocks and reflective only of a couple of overall dimensions an EE might have given some thought to as far as height, length, and width. That’s it. As a mechanical designer, when you design something like an RF housing, you really need to know what those components look like and exactly where they are placed.”

Parts Placement

Once the mechanical constraints of the PCB are set, it is time to bring in the data from the schematic. When the component footprints are imported, they are automatically connected by fine lines to show their pin’s connectivity with other component pins. All these connections are based upon the previously established connectivity defined in the schematic. The imported part footprints usually appear to be piled up randomly off to the side of the defined PCB outline after being imported into database. A design with hundreds of components imported in this way will have so many connections crossed over one another, it will make the pile of parts and connections look like a rat’s nest (which is what it is often called). To a new designer, this state of confusion can appear rather hopeless, but this is where the fun begins. This is the stage in which the designer can begin adding organization to what appears to be chaos. Most designers consider the placement stage of layout their reason for being—they know this first layout step will drive the success of the entire project because parts placement effects every manufacturing process and therefore every manufacturing stakeholder.

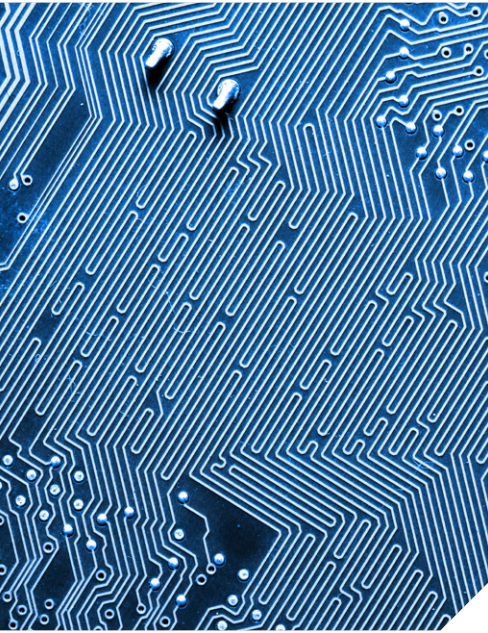


Group Imported Parts and Connections

After the parts are imported, the parts must be grouped. Using the schematic as a reference, a designer can quickly begin grouping the component footprints into clusters of circuits which can be organized so signal connections are at their shortest distance between pins.

A simple tool for navigation and sorting through parts during placement is to set up cross-probing functionality between the schematic and the layout. With cross-probing active, placement of components into groups is made easy. Using multiple display monitors, a quick click on a symbol in the schematic screen will highlight the matching component footprint on the layout screen and make it ready for placement. With the schematic organized with a flow intended to represent the placement of the parts on the PCB, the process of grouping is made easy. You can start by finding a significant part on the schematic, say an input connector; then highlight the connector in the schematic and see the software cross-probes to the matching connector in the layout. Now that the layout's connector footprint is active, it may be dragged over to an area close to where it will be within the PCB outline. Next, highlight and drag any filtering components over, close to the same way you did the connector. During this grouping process, the parts may be rotated to shorten their connectivity.

Many things about the evolving layout will begin to come into view during the grouping phase. Component clusters will begin to show the ratio of component area to PCB area outline. Though the component groups have been organized so their local connections remain short, it becomes clear now the individual groups have connectivity with each other. Many lines interconnecting the groups will eventually be converted into signal traces which will require area. Will all the lines be routed on the outer surfaces of the PCB? Will they fit once the components are all placed? Will more layers be required? These are all questions having to do with layout density which will have to be addressed after determining all the parts will fit within the PCB outline, while still meeting all the stakeholder requirements for Design for Excellence (DFx).



Position Groups onto the Board

Once the components are grouped per the schematic flow, begin organizing the groups. Groups should be organized according to their connectivity flow between each other and to their respective input or output connectors. Pay special attention to the voltage designations in the groups and try to organize similar voltage groups together, envisioning how a voltage plane may be used to connect to all nodes. Are there so many similar connections to single voltage the parts will have to be spread across the board area? Will a single voltage plane be required to cover the whole board area? Or are there multiple voltages assigned to the circuitry which will necessitate the plane layer to be split into multiple sections, causing placement strategy changes for the component groups power pins to contact their respective planes? If this strategy gets too complicated using a single layer, it is easily relieved by adding another dedicated power or ground layer—this however, comes with an added cost.

Design for Test (DFT), Design for Cost (DFC), Design for Manufacture (DFM), Design for Assembly (DFA), Design for Repair, Reuse, and Recyclability (DFR3) and many other “DF’s can be organized and identified into one great Design for Excellence (DFx) concept. During placement it is important to place much focus on DFM, DFA, and DFT.

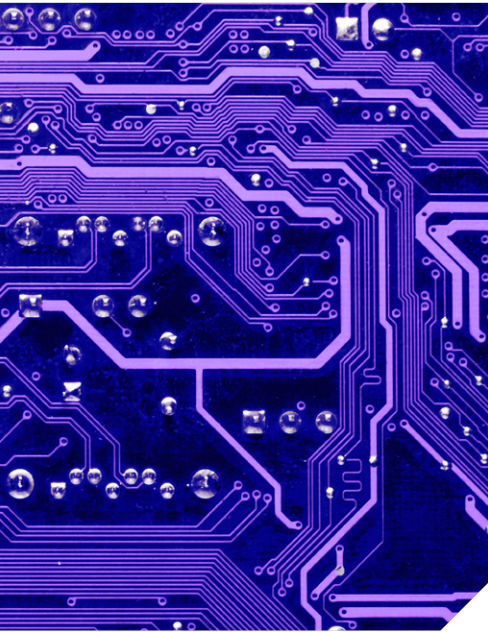
To help see more clearly, assign colors to some of the pins connected to power and ground—this will allow you to turn their rat connection display off, cleaning up the view of the grouped components. Once all the components are in their groups, determine the feasibility of moving the groups onto the PCB outline.

Placement Matters

There are some who say PCB is art, and for this reason, component placement doesn’t matter. While a finished PCB can look like art, saying placement does not matter couldn’t be further from the truth. In our story, Ian found this out the hard way. Placement matters because it affects performance and manufacturability.

For example, ask any manufacturing engineer about the processing ramifications of adding a three-cent chip resistor to the secondary side of the board. They would tell you that would add a relatively immense cost. The PCB would now have to undergo a second side pass through all the same processes which the primary side endured. First, it would require a two-hundred-dollar solder paste stencil and processing for solder paste deposition. Then, manufacturing time would be required for the assembly to run through the pick and place stage. Next, the entire PCB would be subjected to another thermal excursion in the reflow oven. More time would be required to document the secondary side of the board so it could run through the inspection process.

Hopefully all the groups will fit, and the designer can go on to refine the placement. What if the groups don't fit? First, don't panic.



Checking in with a manufacturing stakeholder for wise council on DFM—even for placement of a three-cent chip resistor—can save thousands of dollars in cost and is a far better plan than using “artistic license.”

DFx Tradeoffs—Design Density

It is important to consider design density early in the placement process. If the PCB outline has already been defined by the ME and the BOM has already been defined, using a CAD layout tool is the quickest way to begin this analysis. With the components already grouped, the designer can begin by moving the groups onto the layout. Hopefully all the groups will fit, and the designer can go on to refine the placement.

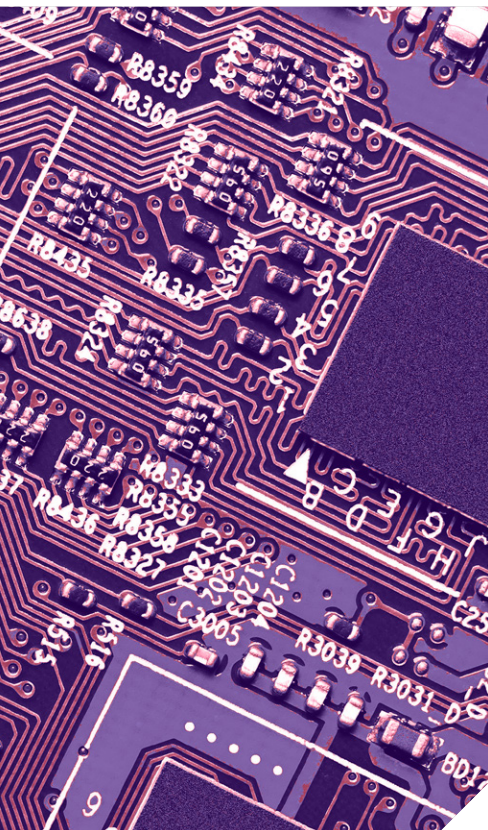
What if the groups don't fit? First, don't panic. A few logical steps can be taken to remedy this. Remember, the component groups are not set in stone at this point. Can placement of the groups be rotated? Can they be stretched horizontally or vertically to fit? At this point, the designer will begin to get an idea for whether all the parts will fit on a single side of the layout or not. If it appears nudging individual parts in the groups will help all the parts to fit, then continue to smooth out the placement. If it is evident the parts will still not fit, then it is time to consider utilizing the bottom (now secondary) side of the PCB.

This is not a step to be considered lightly, as transitioning to a two-sided assembly brings the PCB design into another manufacturing class and will most certainly increase manufacturing costs. Sometimes a designer just gets tired of trying to fight the laws of physics and must switch to a double-sided assembly configuration if the parts simply will not fit on a single side.

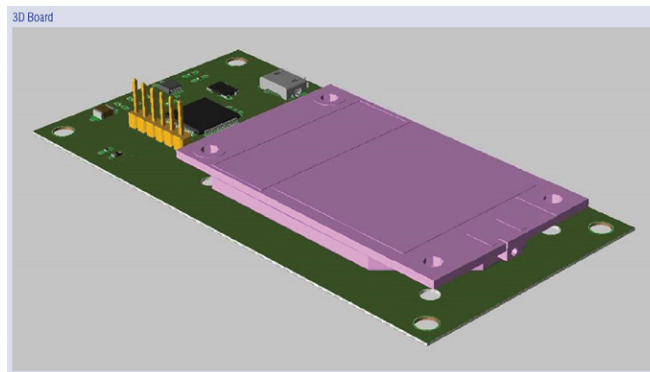
How does one decide which parts to flip to the bottom? This is dependent on component types, their size, how they must perform electrically, and how they must be installed at assembly. Due to these numerous factors, one could produce many possible answers to this question. However, at its most basic level, there are four major areas to consider: Mechanical fit, electrical performance, thermal performance, and assembly.

Placement for Mechanical Fit

As already mentioned, the parts must fit on the given PCB outline in addition to any mechanical fit criteria considerations. The parts must not interfere mechanically with each other. ECAD tools facilitate checking for mechanical interference conditions if the part footprints include a “placement courtyard” geometry on a specific layer. This data is used as the value by which the software can alert for lateral interference, or even dynamically nudge a neighboring component if the two placement courtyards touch. The values for proximity to other components and other design features such as board outlines and drilled holes can be set in the software design rules. Once board-level interference has been checked, at this point it is important to check in with the mechanical stakeholder to check for any assembly interference conditions which



may have been introduced during ECAD parts placement. Design teams rarely have the luxury of freezing the mechanical portion of a project after conveying placement information to the PCB designer. Due to the pace of some projects, MCAD and ECAD portions of design are often leap frogging one another with changes. Collaborative, next assembly 3D checking is often implemented several times during the PCB placement process.



Pro-Tip from Joe Bouza

“Overall, the key to success in all disciplines of design is effective, dynamic collaboration. Collaboration is a process. Nowadays, ECAD/MCAD is challenged with defining constraints for electronic components that have sizes less than a grain of sand and for machined chassis and enclosures which must keep out aggressive energies.”

Placement for Electrical Performance

Grouping components is only an organizational method for preliminary placement. Single-side grouping only addresses basic, lateral proximity to related components. With some part packages, access to the electrical pin is impeded by the component outline; causing the pin to be moved far away from its required destination. In this case, flipping a component to the far side can help electrical performance because the part pins can now be located close without the component bodies interfering.

Component body size prevents its pins from being located close to other parts

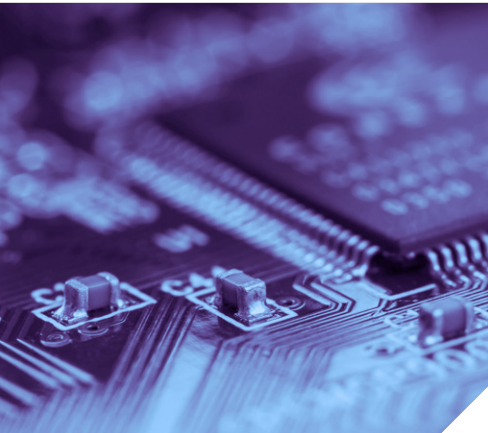


For digital areas of the layout, consider power distribution first. It is important to locate digital components so they will have access to reference power and ground planes located directly beneath. Locate the bypass and decoupling capacitors close to device power pins for best performance.

Layout of the digital portion may include consideration for parts known as crystal oscillators to control the timing of the circuitry. It is very important to locate crystals close to the devices they will control so the length of their “noisy” connections will be kept as short as possible.

Regarding analog components, keep their groups separate from digital circuitry. It is important to consider a performance goal for analog placement and keep routing of the connections short.

If the time and materials it will take to put the PCBA together exceeds the target sales price of the PCBA, the project will indeed be doomed.



Placement for Thermal Performance

Due to power requirements and function, some components can run hot—it is important to mitigate this heat and direct it away from the PCB. Heat can cause many problems for an operating PCBA due to the many various materials used and their different rates of expansion (coefficient of thermal expansion). Concentrations of heat on a PCBA can cause the PCB to expand dramatically in its Z-axis because of a lack of constraining materials to prevent it. High heat from an overdriven LED in contact with a multi-layer PCB structure supporting nearby vias (discussed in detail in the PCB routing section) can expand the supporting material enough to “pop” the via, causing failure. Components which will be dissipating heat will need to be managed by the engineer working with the mechanical engineer to make sure the assembly has a way to conduct or convect the heat away from the PCB.

A few placement considerations for hot components:

- Add a copper plane underneath and in contact with the component to provide a conduction path for the heat away from the part. Extend the plane out far enough to allow the copper plane to sufficiently convect the heat into the air.
- Add a mechanical heat sink to the component to convect heat away. Component heat sinks are readily available for many parts and come in many shapes and sizes.
- Avoid concentrating hot components together—spread them out. Locate hot components in the path of airflow from a fan in the assembly and be wary of larger components blocking airflow.

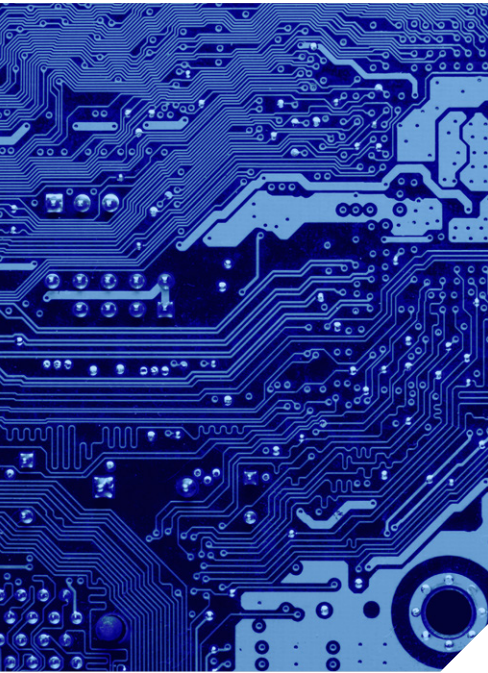
Placement for Assembly Constraints

After considering placement options for mechanical fit, electrical performance, and excessive thermal conditions, any of which could doom the success of the PCBA if not mediated, final consideration for how the part will be successfully assembled onto the PCBA must be merged together with all other constraints. Even if the PCBA will fit with all mating parts, performs flawlessly, and runs as cool as can be expected, it will still be doomed to fail as a product if it cannot be reasonably assembled. Remember, the assembly stakeholders measure ease of assembly in units of time and materials. If the time and materials it will take to put the PCBA together exceeds the target sales price of the PCBA, the project will indeed be doomed.

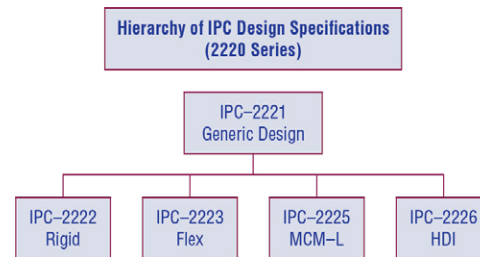
So, what can a designer do during the placement phase to increase performance and reduce time and materials cost?

There seems to be a lot of information out there regarding many unique aspects of PCB design. Over forty-two design for manufacturing guidelines have been put together by EMS providers with various takes on how parts placement can be accomplished for their own internal processing. These guidelines contain valuable information if you are doing business with a select supplier. Designers need to know where their towel is, so to speak. However, there are just as many circumstances in which using a guideline for implementation at one EMS provider might be insufficient, or down-right inappropriate, for another. Rather than attempting to describe a galaxy of assembly conditions and circumstances affecting placement decisions here, we'll give a nod to the IPC. The IPC organization has been in the business of bringing PCB stakeholders together for many years. The organization

It is important to understand the importance of establishing and cultivating design and manufacturing contacts.



has published a key specification, the IPC-2220 generic design series standards. IPC-2220 includes a fine section on parts placement for a myriad of assembly processes which have been endorsed by a diverse association of electronics industry representatives.



Component placement for DfX requires a depth of knowledge not only with regard for the component materials and their physical properties, but for how the components will operate with other components in a circuit and how they will need to perform in various operating environments. Any designer working on a complex PCB will eventually need to make decisions of compromise between some of the opposing forces of DfX.

For instance, when considering design for electrical performance constraints, an EE may dictate the location of a capacitor pin must be placed within .025 [0.64] of an IC's power pin. However, this constraint will clearly conflict with a design for manufacturing constraint from the assembly manufacturing engineer who needs clearance between pins for wave solderability.

In this example, the two forces of electrical performance and manufacturability have collided and require resolution. Can the capacitor be moved to the opposite side, and soldered by reflow? Can the soldering operation shift to a selective method rather than a wave?

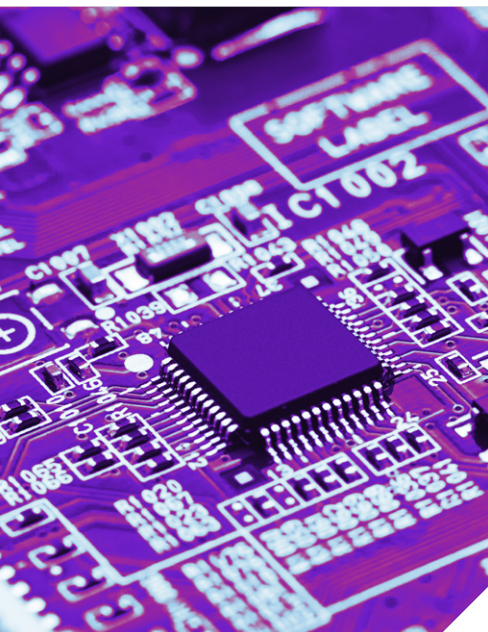
As a champion of DfX, it is the responsibility of the PCB design engineer to bring the two stakeholders together and negotiate compromise. DfX does not mean every process will be perfect. DfX means the requirements of all stakeholders have been considered and the design has been optimized via stakeholder consensus.

Shaking hands with Your Network

It is important to understand the need for establishing and cultivating design and manufacturing contacts. Expanding your professional network will benefit you in the long run. There will always be design challenges and when required, turning to your network will help you to come up with the best possible answer.

The PCB design engineer's responsibility is to combine front-end project information with the mechanical engineer (who provides the PCB outline) and begin the PCB layout. It is important for PCB design engineers to use a consistent process, always carefully examine the schematic and BOM, and look for any special notes, or anything non-standard, on the schematic before starting the layout.

Getting in touch and asking questions about the schematic beforehand is appreciated by all stakeholders. By doing so, you might bring up a question they may not have thought of. Establishing this early in the design process allows involved stakeholders to modify information before the PCB design gets started.



Working with the ME Stakeholder

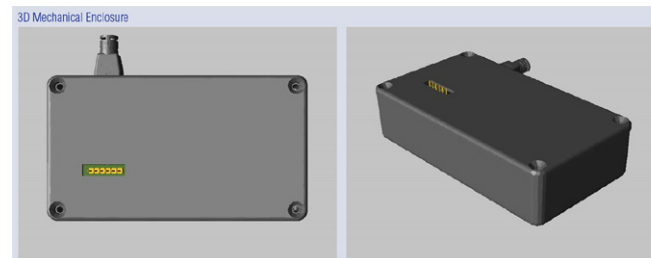
A mechanical engineer can only guesstimate the board area required for the layout. Rarely is a complete schematic and BOM accessible to the ME while the outer packaging of the product is being designed. Early in the mechanical design layout phase, the ME will usually have access to interface components, like connectors and switches, and will naturally define a PCB outline based upon the area left over, after the mechanical design is complete.

Pro-Tip from Joe Bouza

“The workflow I am seeing is still pretty traditional where the mechanical design is solidified first. However, I am seeing a collaborative trend in which the PCB already exists, and there is a requirement to design a housing around the PCB. What we are describing here are two methodologies: designing from the outside in or the inside, out and there are benefits to both. The mechanical designer sees the requirements of the outside world. However, as the design progresses, there is a need for the ECAD designer to push back and let MCAD know what works and what doesn’t work regarding electrical performance and part placement requirements. We’ve come a long way with being able to trade mechanical placement requirements back-and-forth using STEP files. This CAD technology has made it much easier to collaborate. However, we all must remember when we are communicating with STEP files, we are sharing absolute mechanical values. Tolerance is not reflected in the STEP files.”

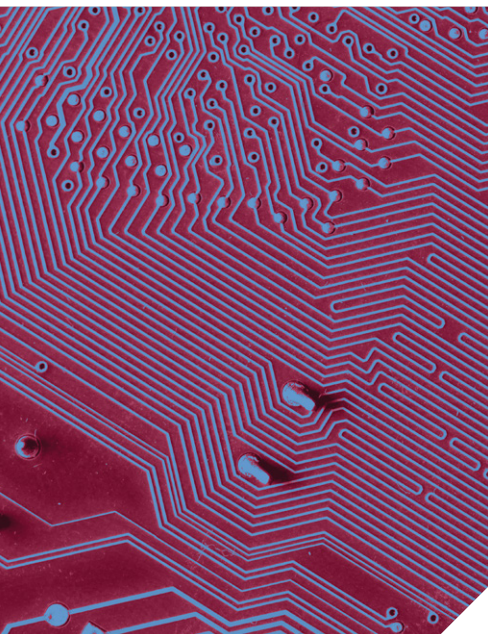
Cross-checking tools and placement

Using the ECAD tool is now easier than ever to cross-check PCB layout with mechanical layout. ECAD and MCAD tool industries are on convergent paths which someday will merge to become one. While rapid progress is being made, current projects are still designed by separate mechanical and electrical stakeholders who must be well-versed in communicating their perspectives.



Pro-Tip from Joe Bouza

“The capability to trade placement conditions early in the design is key to shortening the design cycle. This requires quick, iterative collaboration. Dogmatic placement requirements from one side or the other just do not work. With dense packaging requirements today, it is too easy to get both sides backed into design corners where the design cannot move forward unless they move together. It is natural for an ECAD/MCAD team to go through three iterations during placement. If this collaboration is done early, using the basic known constraints—grouped circuitry defined, mounting holes defined, and then board outline, for instance—the remainder of the ECAD/MCAD communication is smoothed out.”



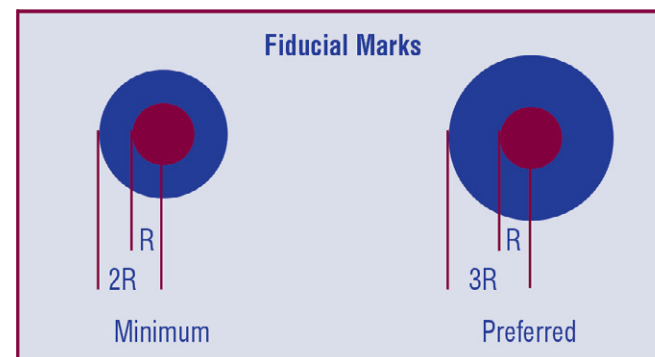
Working with the Assembly Manufacturing Engineer Stakeholder

Once the placement is finalized and has been reviewed internally by the EE and ME, it is a very good idea to invite a review from the assembly stakeholder. Most EMS providers are happy to perform this review, but they will require the appropriate data to review effectively. It is important to call and ask what data they need. Most likely, the EMS provider will be very happy to receive the layout in ODB++ or IPC-2581 formats. An assembly drawing (unfinished or not at this point) will provide workmanship standards and peripheral information which may be used for the review.

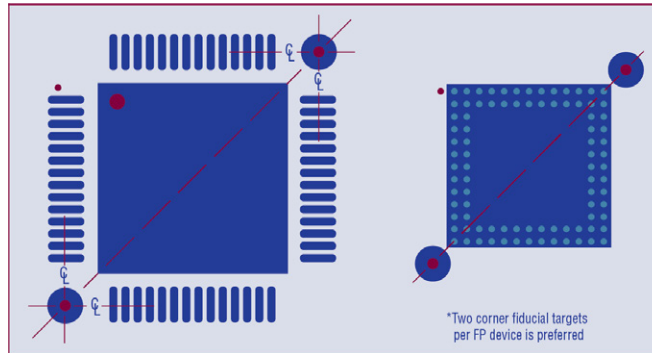
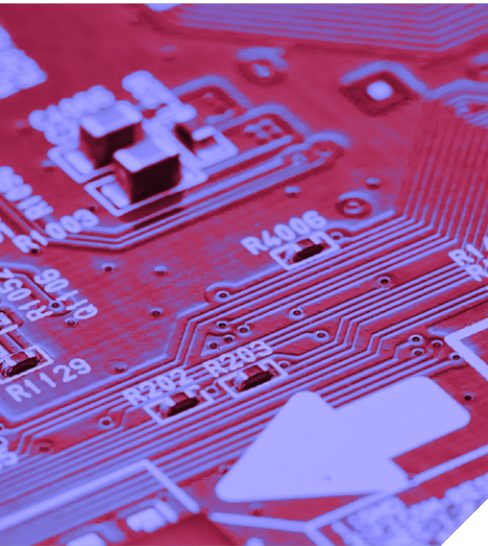
Fiducial Marks

Fiducial marks are commonly used in PCB manufacturing to aid machinery and processes equipped with Automated Optical Inspection (AOI) technology. When fiducials are incorporated into the design layout, the machinery can use them to locate and orient specific points on the PCB for positioning or placement of parts by methods of triangulation. Fiducial markings may be of most any shape, but the sizing and especially the contrast the fiducial has with its surrounding topology is important.

Most AOI equipment can easily detect a .040[1mm] diameter fiducial etched in copper if there is at least some clearance around the shape. It is common to clear solder-resistant material (or any legend marking) by half the diameter of the fiducial (commonly referred to as 'fid'). It is very common to create a fiducial mark as a padstack structure using a pad on the first layer with a solder-resist clearance of .020[.51mm] in the design layout. Once the fiducial is created, place one in each far corner of the PCB (minimum of three corners) for surfaces which will be populated with SMT components.



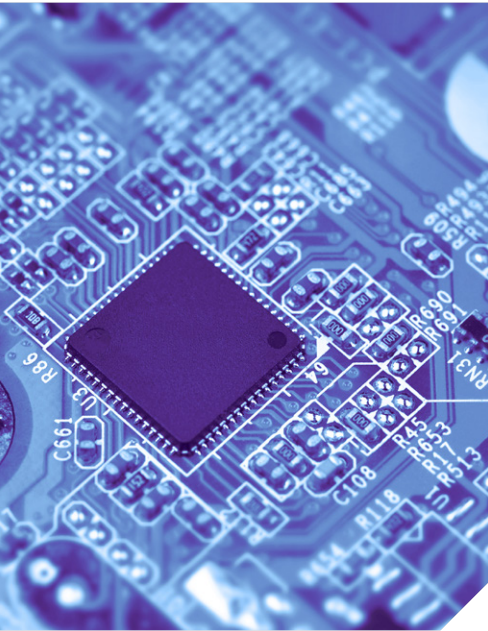
PCB component footprints are like the bricks of a building—they must be strong and pure.



Sometimes a supplier will request “local fiducials” be placed at the corners of fine pitch, high pin-count parts to leverage the technology to place them more accurately. When placed off board, onto the rails of a manufacturing panel, fiducials can serve to designate ‘stuff’ or ‘no stuff’ options on a PCB assembly. Sometimes individual PCB panel images do not pass inspection and are marked by a large X. Since the remaining PCB images are good, by simply covering the fiducial of the X’d out PCBs, the assembly equipment will ignore the failed boards and only assembly the good ones.

Conclusion

The steps for placing components onto a PCB layout are very similar to those which would be followed by a construction company designing a house or a city. Successful completion of either requires an investment of time and planning. PCB component footprints are like the bricks of a building—they must be strong and pure. They must be located near the site for easy access. Setting up the layout parameters of a PCB are like conditioning and leveling the ground at the building site before the heavy work begins. Defining the mechanical constraints of a PCB is comparable to drawing up building plans which inspectors must approve before the project can move forward. By taking this simple metaphor to an extreme, it is easy to see the steps involved in placing parts onto a PCB design layout could be considered a lot like the steps involved in architecturally planning an urban construction project. However, keeping it simple by following the rules, determining where compromises must be made, and bringing together to right people for effective collaboration is a proven strategy for success in any scale of project, in any industry.

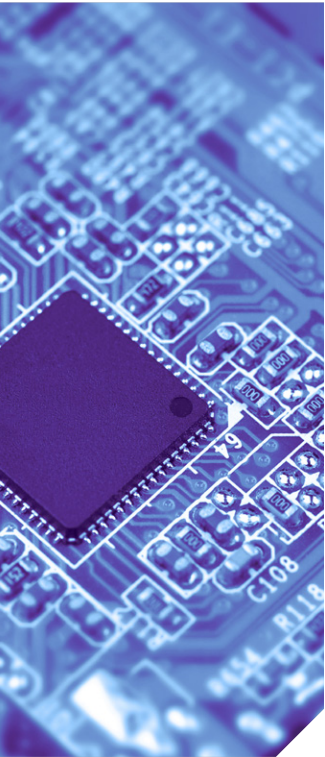


Tips for Placing Parts:

- ☐ Considering the PCB layout is only performed once, and the manufacturing process dictated by the PCB layout can be performed millions of times, Design for Excellence (including design for Fabrication, Assembly, and Test) must be considered during placement.
- ☐ Color code nets in the layout based on their node count and their criticality. Once color coded, the rat's nest display for high node count nets (like PWR and GND) can be shut off, allowing better visibility of remaining signal nets.
- ☐ Group components together off-board; primarily based upon their functionality with shortest distance between signal and power pins, and secondarily how they are shown in the schematic.
- ☐ Generally, distance between GND connections do not have to be kept short, but will need to connect to a robust GND path, or ideally, a plane.
- ☐ Once grouped, begin moving the mechanically-fixed components onto the PCB. Fixed location input connectors, output connectors, and any other interface components (like switches and even some LEDs) have priority. Check for collisions with other fixed keep-out areas—sometimes mechanical engineers only account for component pins and don't allow for larger soldering lands.
- ☐ Once fixed components are located, lock them into place.
- ☐ Move component groups into place. Tight groups may now have to stretch and bend to fit around keep-outs and other groups. Prioritize this movement to have least effect on the original group.
- ☐ Smooth out the placement in consideration for DfX. Aim for similar rotation of like components to help manufacturing and inspection.
- ☐ Consider balancing out the spacing between less-critical parts at this point such as adding spacing between components for better routing, future test points, automated placement, heat profiling, and inspection.
- ☐ In many cases, all groups will not fit on a single side of the PCB layout. In this case, prioritize movement of parts. First, similar discreet parts (CAPS, Resistors) or some components may have to rotate and move to the secondary side of the layout.

Chapter 6

DFT for In-Circuit Test and JTAG



The success of the manufacturing process is based upon the successful execution and ability to measure the health of each process step. The machines on assembly lines install thousands of parts every minute; therefore, throughout the assembly process, manufacturing checks must be completed. These checks verify many important items pertaining to assembly manufacturing. However, final testing—in-circuit testing capability—must be designed into the PCB at the layout stage. DFT allows capability for testing which includes component connectivity, electrical value, and proper component orientation.

Types of Testing

AXI Post Wave Inspection

AXI Solder Joint Inspection

In-Circuit Testing

AOI Post Wave Inspection

AOI Component Measurement

AOI Solder Joint Inspection

AOI Solder Paste

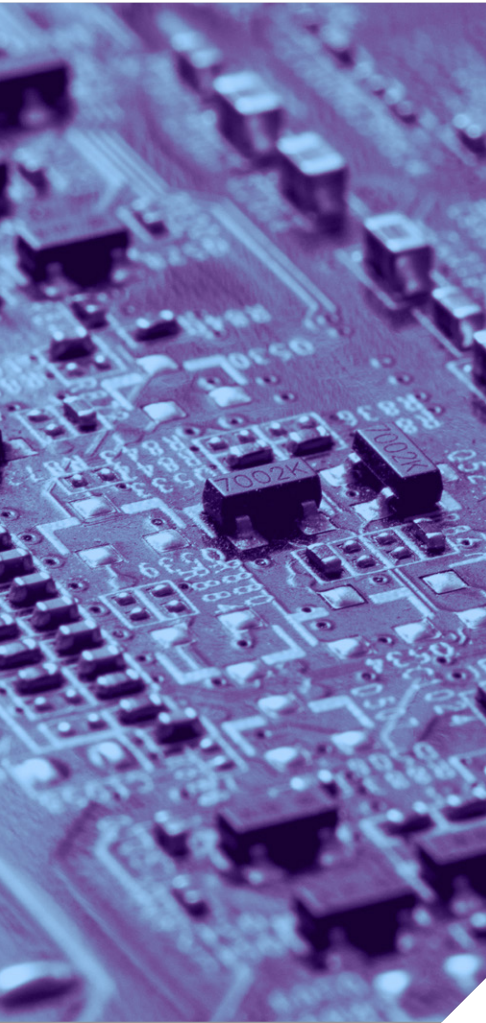
Functional Test

Many of these tests can be run without required modifications to the PCB layout; however In-Circuit Testing (ICT) does require some additional features added to the PCB, so this will be the focus of this section.

Remember how the virtual production of Ian's first PCB design went? How it looked good on screen, but as the assembler could see, there were just too many test inconsistencies with the BOM, the part footprints, and the routing. With only the non-intelligent Gerber file data provided (and no test points included) it was impossible to test Ian's design. Critical defects were not detected along the way.

Test engineers understand production test fixtures and the development of testing software can get expensive. Incorporation of simple DFT for ICT basics (such as bed-of-nails testing for single-sided testing or clamshell fixtures to test two sides of a PCB assembly simultaneously) can greatly help assembly teams to check and verify their production work. This allows parts which pass the electrical tests to move on to their next production phases with zero defects.

Like Ian, you might be left asking yourself: "Should I have taken the time and spent more money incorporating DFT for ICT?"



Test Points

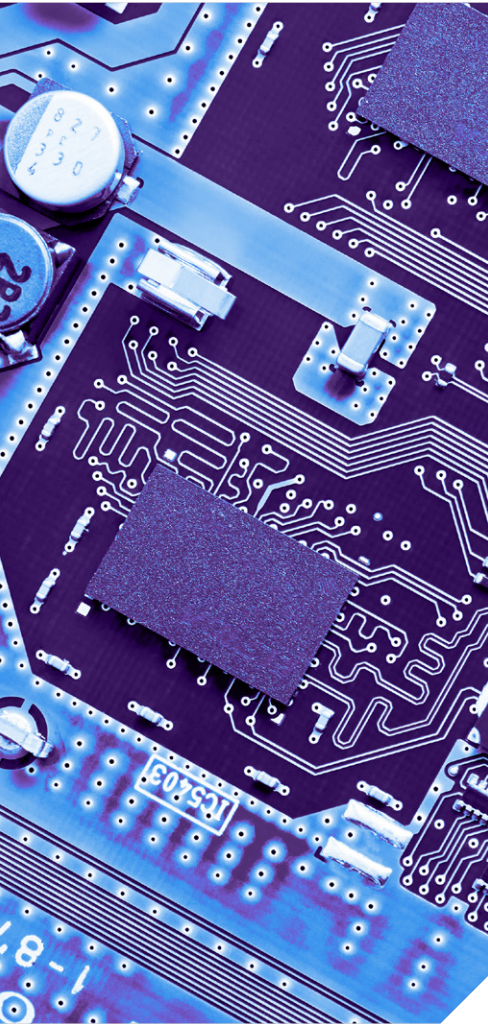
Test points are etched target shapes which include short routes making electrical connection to the circuit nets of the PCBA. Test points are typically round, .035 [0.89] or larger and are cleared of any solder resist or legend ink which would impede electrical connectivity when coming into contact with a test probe. Test points can be added to the schematic and even include reference designation if required. In many cases, if testability is called for at the beginning of a layout project, the EE will work to address the requirements into the layout at the time placement, prior to routing. With dense designs it is far too difficult to try to wedge test points into a routed bus after the fact. Test points can be used by the test engineers to verify the continuity and performance for every connection on the PCBA. This capability is a very powerful tool when looking for manufacturing defects on an assembly. With test points added, a test engineer can check for backward installation of polarized components like caps or diodes. Damaged components can often be found and misplaced components with incorrect values can be audited for.

Test point quantity requirements can vary based upon the test methodology. Requirements for a PCBA which employs JTAG (which we will talk more about later) test will only need a few access points. However, if full testing is required on a PCBA without JTAG, it is very common for test engineers to require at least one test point per net, except for power and GND which should include many test points sprinkled about the PCB for adequate access.

As mentioned, test point strategy is usually determined at the time of parts placement. If test points are going to be added to every net, a test point routine will be run which automatically adds the test points. Once the routine is run, the test points will usually be added off-board in the layout. The test points can then be moved into place by the designer manually. Before placing test points, a designer should pick a single side of the PCB to be designated as the DFT side. It often makes a lot of sense to choose the secondary side of the PCB to be the testable side. The secondary side is usually the side with the least amount of parts and therefore the most accessibility. Spacing the test points sufficiently is paramount to good DFT. Test point spacing of .100 [2.54] is considered good by the test engineering stakeholders because such spacing allows for least expensive test probes and ideal ease of access. However, real world design density will not always allow for such robust spacing. In this case, reducing spacing by .025 [0.64] -- .100, .075, .050 -- grid spacing is considered acceptable though the smaller spacing will yield a higher cost fixture.

There are many factors weighing into the decision of whether to include DFT for ICT into a design layout.

Adding test point coverage to critical signals can endanger performance due to "stubs" which are often created when adding the extra trace length required when connecting to an optimally placed test point. Depending on how DFT is incorporated, cost can have a direct effect upon the manufacturer's profitability which can affect the customer's profitability, and that will without a doubt affect the consumer's wallet.



It is no secret DFT for ICT can get expensive as there are many parts of the process which add cost:

- PCB Design Engineer time—schematic and layout
- Test Engineering time
- Software Engineering time
- Building of the test fixture

All these resources and equipment can add up. So an engineering team must be in touch with several attributes of the PCB before deciding to add DFT for ICT. If the team can mark all the following “DFT required” checkboxes when making their analysis, the expense up-front might be considered an investment. Let’s list some of the basic reasons which can justify DFT for ICT:

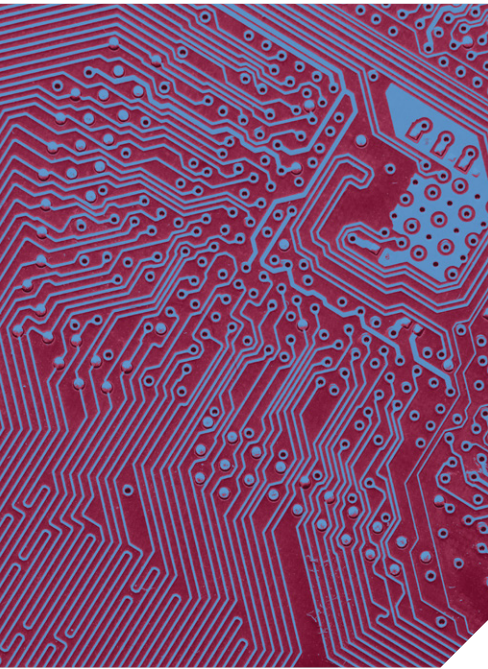
- Provides probe access to nets on the PCBA which would not be accessible otherwise for testing and analyzing signal performance.
- In production volumes, tracking and measurement of the PCB processes is the key to profitability.
- ICT can detect shorts, opens, lifted leads, and missing parts.
- ICT can detect dead parts, wrong parts, and bad parts.
- ICT can check for inverted polarity and even missing, socketed parts.

Considering materials and time, PCBs which have ridden the conveyor far into the assembly process are worth quite a bit of money if they have been assembled without defect. Checking for defects like those listed above with automated, in-circuit testing at the completion of the assembly process confirm the quality of the assembly and therefore confirm its value. However, the value of a PCBA with even one defect, such as a misplaced resistor, drops to zero.

AMEs do not want to scrap an entire board due to a single defect, so usually they will set the defective assembly aside and rework it manually later. Catching and tracking defects during individual assembly processes helps AMEs to see if there are any defects which are occurring consistently to any one part. For instance, if the same part is failing consistently on a run of PCBs, manufacturing engineers will perform a root cause analysis on the condition. For example, they may find an imbalance of copper mass connected to the component’s land causing inconsistent cooling between them. This is just one type of defect that can be detected.

There are hundreds, if not thousands, of other defects which can be caught by incorporating test capability into the design layout. Incorporating DFT for ICT into a PCB layout can take time and add cost up front. Many ask the question “Why do I have to pay for a test fixture whose only purpose is to check the quality of the EMS supplier? Isn’t quality their responsibility to check?” Yes, quality always falls in the lap of the EMS provider, whether building a limited run of 100 PCB assemblies or 100,000. However, the answer to the question is a matter of cost. Measuring quality on a run of 100 PCB assemblies will most likely be accomplished manually. If it takes a matter of 30 minutes to test the PCB manually, the cost for testing the run would be calculated at 50 hours at a rate of say, \$100 per hour

Generally, adding a single test point per net on the PCBA design if possible, makes the test engineering stakeholders happy.



for a total cost of \$5000—far less expensive than investing in a test fixture and implementing DFT for ICT. However, to apply a manual test strategy to 100,000 would take 50,000 technician hours costing five-million dollars. To apply manual testing to such a large run of assemblies would lead to a doomed schedule and financial ruin. This exaggerated example is the reason one might opt to pay for automation. DFT for ICT reduces testing time to seconds and therefore saves overall cost even after investing in test equipment.

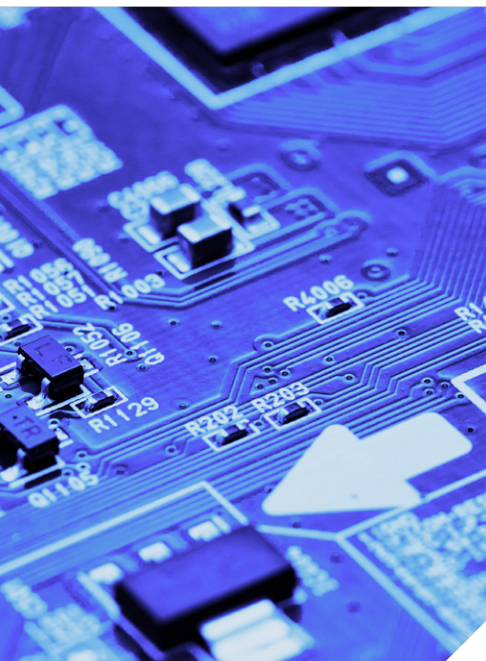
It's important to remember a test strategy must be clearly developed to identify goals, cost, quality, and scheduling. Be clear regarding which nets will need to be accessed, whether this is through a note or adding test points to the schematic.

The general requirements for adding test points to a PCB layout are simple: test points are ideally added to the non-component side of a PCB. However, if the side selected for test points includes components, avoid placement near parts taller than .200 [5.08mm]. Common test point shape and size is circular, with an ideal diameter of .040 [1.00]. This diameter ensures the spring-loaded test point probes will be placed accurately enough to raise the probability of contact to the test pads to 100% per 1000 hits. If there is limited space on the layout, test point size may be reduced slightly to .035 [0.89]; however, reducing the diameter beyond that will increase the probability of a probe miss significantly. Generally, adding a single test point per net on the PCBA design, if possible, makes the test engineering stakeholders happy. Also, it helps greatly if many extra test points can be added to ground and power across the PCB for ease of access.

When implementing DFT for ICT, it is important for the PCB design engineer to understand once the PCB is manufactured and a test fixture is built, any future changes to the PCB should not disturb previously placed test points—it is recommended they be locked down in the design. While it is easy to move a test point on a layout, it is very difficult and expensive to re-tool a test fixture to match the change.

The Surface Mount Technology Association (SMTA) has published TP-101E Testability Guidelines. This comprehensive guide is a great go-to which should be read by all project stakeholders to better understand our test engineering counterparts. This guide should interest PCB designers because the publication lists several general guidelines for creating test equipment for the board you've designed. In addition, the guide describes 32 probing-fixture guidelines which the test engineer must adhere to.

[Click to Enlarge](#)



JTAG

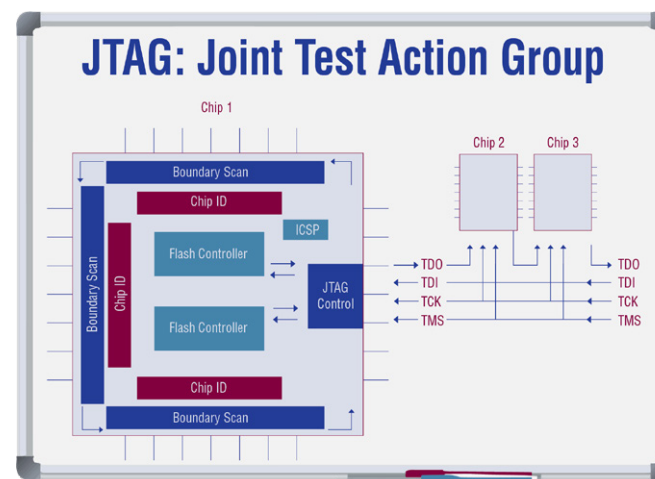
What if there is just no room on the PCB layout to add so many test points. Is there another option? In an ideal world, an excellent scenario for a test engineer is to be able to set up a test routine for a PCBA design to include at least one test point per net. However, this is not always feasible.

Pro-Tip from David Ruff

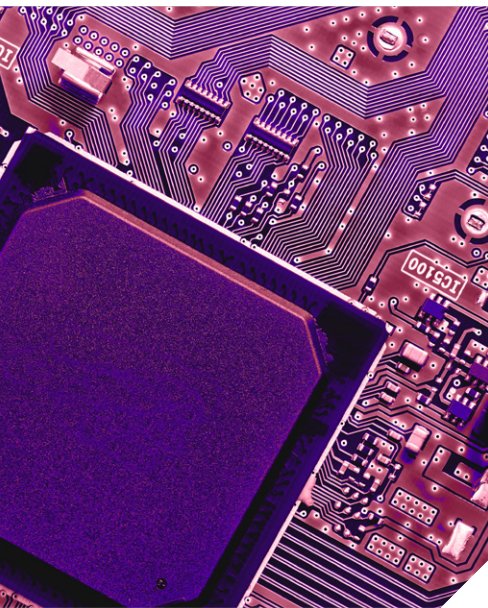
It helps the test engineer greatly if power and ground nets have many test points connected which are accessible across the PCBA, but most PCBA designs I see never come close to that requirement.

With high density requirements on PCB's continuing to rise, having enough real estate to add test points for 100% testability on a PCBA is a rarity. Implementing partial test point coverage can make some test engineers cringe and ask, "if you're not fully testing, why test at all?" Missing test points on a PCBA with no physical space remaining is a weak compromise. However, there is another option in this circumstance brought to us by the good folks at JTAG—which stands for Joint Action Test Group.

JTAG was formed by a group of companies in the 1980s to define some extra silicon which would be added to the workhorse chips on your board. This extra silicon would then allow devices to be put into a 'test mode' giving you control of the pins on the device. It is very similar to another common test protocol, 'Boundary Scan,' both of which are governed by IEEE 1149.1-6. Note: All main devices on your PCBA—processors, FPGAs, CPLDs, and BGAs—should include JTAG.



The design database can be set up to audit each net for testability.



The JTAG test spec defines which signals need to be accessed. A PCB design engineer needs to be aware there is a minimum of four-wires. The signals used are:

- TCK (Test Clock) – this signal synchronizes the internal state machine operations.
- TMS (Test Mode Select) – this signal is sampled at the rising edge of TCK to determine the next state.
- TDI (Test Data In) – this signal represents the data shifted into the device's test or programming logic. It is sampled at the rising edge of TCK when the internal state machine is in the correct state.
- TDO (Test Data Out) – this signal represents the data shifted out of the device's test or programming logic and is valid on the falling edge of TCK when the internal state machine is in the correct state.

There is an optional signal which can be added: TRST (Test Reset), which when available, can reset the TAP controller's state machine.

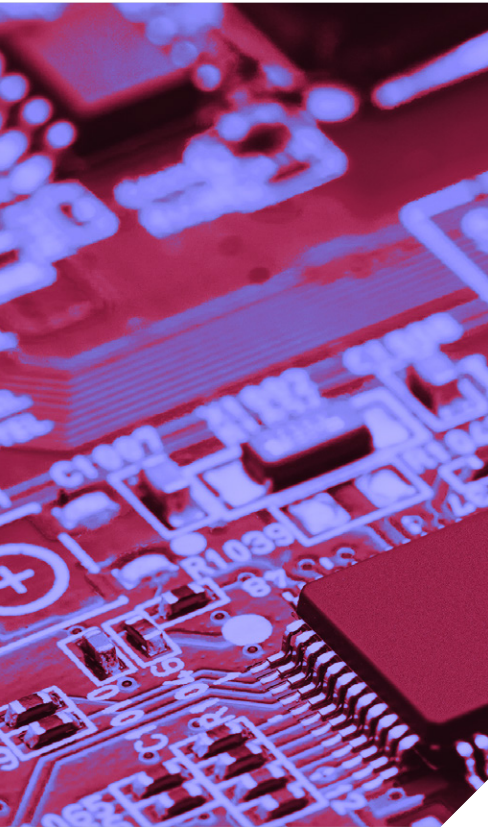
Pro-Tip from David Ruff

The 1149 specification defines these signals and how they operate, but it does not define a connector size or shape. So, a design can use most any connector available or even a few test points placed onto the PCB to make connections to these signals and employ JTAG.

Conclusion

When is the best time for considering DFT? As I've learned in our story, test engineers are important stakeholders in any PCB design project which will be going to volume. They should be contacted early on and invited to the project stakeholder meeting. As circuit performance requirements are being defined, questions about how performance will be tested and verified do not naturally come to mind for other project stakeholders. Test engineering must be provided schematics and brought to the table at the beginning of a project to address whether testing is required, what equipment will be used, and provide estimates for initial cost.

Once the decision is made that testing will be required on the PCB, DFT can be implemented during the layout phase of the PCB. The design database can be set up to audit each net for testability. The software should be able to export a DFT report showing all net names with respective test point XY locations which can be of great use to the test engineer when creating a fixture. This design for test practice ensures the best chance for all testing requirements to be successfully included into the design.

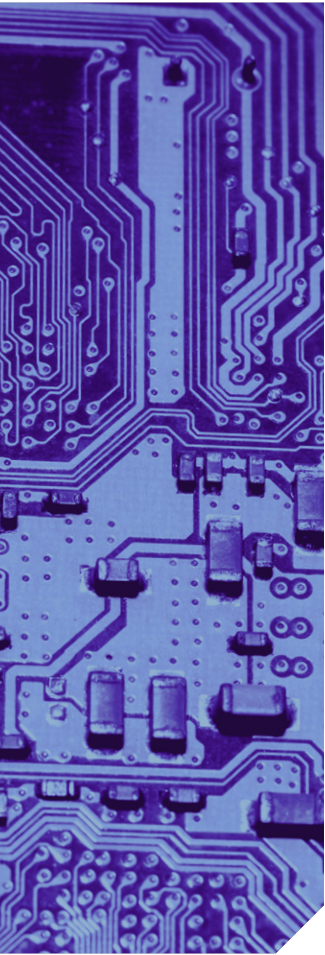


Checklist for Incorporating Design for Test Into Circuit Testing:

- ☐ Coordinate the test group at the start of a project to determine the production volume of the project and the test methodology (JTAG, in circuit, or functional).
- ☐ Become familiar with IEEE 829 and IEEE 1149 test methodologies.
- ☐ Make every effort to design test access to a single side of the PCBA.
- ☐ Make test point lands .035[.89mm] round minimum.
- ☐ Strive to space test point lands greater than .100[2.54mm] apart. TP lands can be closer .050[1.27mm] with significant cost increase.
- ☐ Strive to add at least one test point per signal net for address, data, and bus lines. More can help testability access, but avoid creating “stubs” or extra copper mass added to consistent signal trace geometry.
- ☐ Sprinkle power and ground access points liberally and consistently across the layout.
- ☐ Avoid placing test points close to taller components over .200[5.08mm].
- ☐ Set up your design database to audit each net for testability. The design database should be able to export a DFT report showing all net names with respective test point XY locations which can be of great use to the test engineer when creating a fixture.
- ☐ When placing SMT parts, add fiducials on the same side to assist the downstream assembly processes. Check in with the assembly stakeholders to find out if local fiducials may be required.

Chapter 7

The PCB Design Stackup

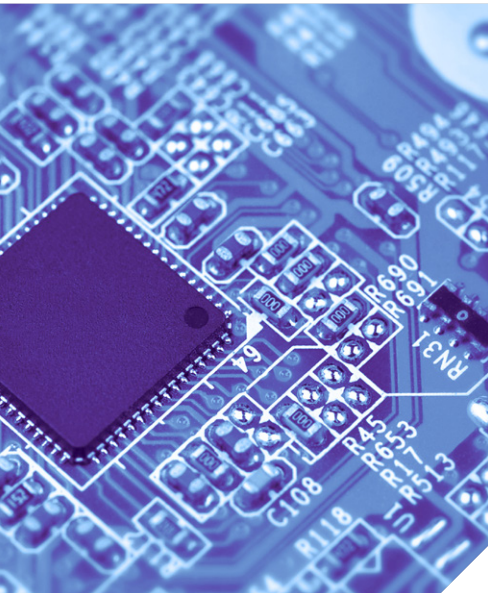


Now that your parts are placed and your test strategy defined, perhaps you are not seeing enough room left over to route traces and create power paths—don't panic. This is a very common condition caused by today's dense packaging. Your design requirements have transitioned into a need for multi-layer PCB design technology, and with that it is time for some vertical thinking; time to consider some important Z axis strategy for routing and power planes.

The term “topology” in the context of a PCB layer refers to geometric properties—copper shapes, clear areas—left over for routing or flooding with more copper. After placement of the components, which may have taken up one or both outer sides of the layout, a designer can see more clearly how much space remains for routing. With some experience and a keen eye to see enough remaining room between part footprints, a designer will be able to begin thinking about whether the connections will be able to be reasonably routed on the two outer layers. Quite often, advanced designers will set up and utilize the software's auto-routing capability to run a feasibility check for routing density. If it appears there is enough space to complete the routing, the PCB will most likely become a two-layer board (IPC class 2) design.

However, if the component footprints occupy most of the area defined by the outline, the layout is most likely too dense to complete the routing on the outer layers. At this point, a multi-layer design configuration must be considered to provide additional layers of copper to complete the routing.

Modern digital circuitry speed is measured in GHz and most, if not all, design requirements have had to change to address it.



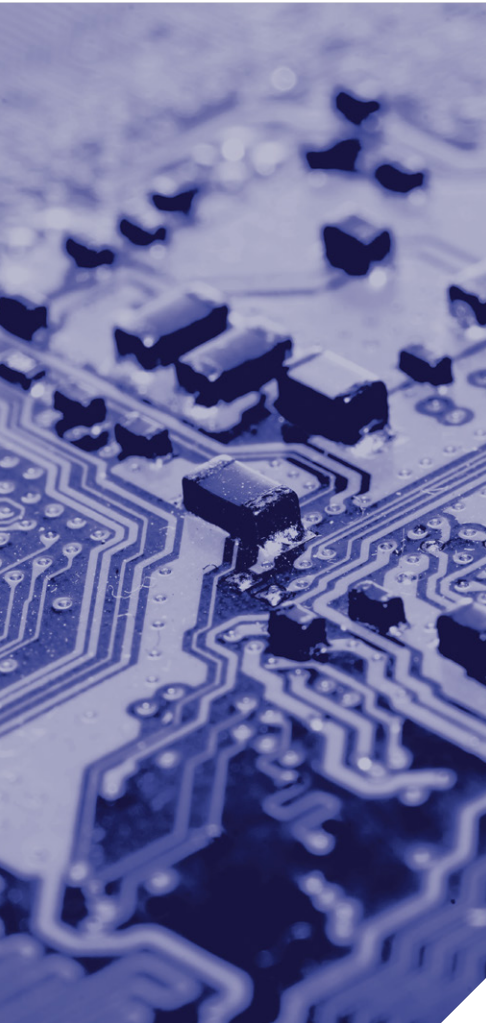
From Two to More

The term “stack-up” refers to the composition and layering order of the materials used in lamination of the PCB. The PCB stack-up is usually documented on the fabrication drawing as a diagram which serves to provide the manufacturer with a quick view of the construction of the PCB. It can then be easily compared to the print, etch, and electrical performance requirements of the PCB.

Selecting a sound PCB stack-up strategy is important because where the etched and plated layers are positioned and laminated from top-to-bottom will not only affect the PCB’s electrical performance, but its mechanical performance as well.

Back in the “old days,” electronics ran at much slower speeds than they do today. Back then, connection lines could run circuitously all around the outer surfaces of the PCB without effecting signal integrity. In fact, a designer could claim bragging rights if a board could be routed in this manner without using vias. Modern day circuit speed has increased exponentially, and the routing methods of yesteryear simply will not work on modern designs. Modern digital circuitry speed is measured in GHz, and most, if not all, design requirements have had to change to address it.

Clock speed, edge rates, rise and fall times, and prevention of unwanted electromagnetic interference (EMI) are all considerations that a PCB design engineer will have to address at some point. These issues are best identified early in the schematic stage as we have mentioned in the previous chapter. Once these constraints are identified, a designer may use a basic field solver or off-the-shelf impedance calculator to determine trace widths and spacing to be used to meet the design for impedance requirements. At the start of the layout, the designer should do a feasibility check with the supplier to select trace widths for impedance-controlled lines; be sure to validate the values in the stack-up. Designers should use care when adding information to the stack-up detail regarding three of the four variables mentioned above. Finished copper thickness is a very important consideration regarding the various conductors’ current-carrying capacity. However, the values of trace width, distance from reference plane, dielectric constant of the material (ϵ_r), and material sources should be allowed to be adjusted by the supplier. Using the stack-up detail to ‘document’ the recipe for a successfully performing PCB prototype sets up a design for procurement challenges. This is because materials used by local prototype shops are often not readily available off-shore.



When considering a stack-up configuration, a designer should be aware of the cost associated with the manipulation of the stack-up parameters to make the best decisions regarding routing density and power distribution. It is important to note here that a project manager, along with the team of stakeholders, have already set many of the design and manufacturing goals for the PCB, which are translated into the term, “constraints,” by the time the project has moved to the layout phase. As the PCB moves to layout, two classic, diametrically opposed constraints need to be sorted out by the designer: design constraints vs. cost constraints. Design constraints define the performance of the electrical attributes of the PCB and usually are associated with increasing quality of materials and layer count. However, cost constraints define the profitability of the PCB. From the project stakeholder’s overall viewpoint, it can be well-stated that without intelligent adjustment and compromise to effectively meet both constraints, there is no product.

Knowing certain “cost adders” related to PCB stack-up will help the designer to make critical decisions while considering appropriate cost vs. performance compromises for the layout.

PCB Stack-up Cost-Adders

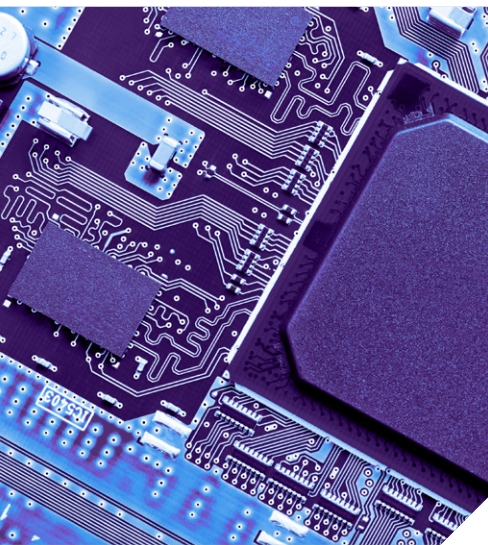
Cost of Copper Thickness

The story about how copper foil thickness came to be referred to in ounces is an interesting one. In short, the reference to copper thickness was derived by how much one square foot weighed when being sold to the tinkers and workers in the roofing industry. For a PCB design engineer, the weight of copper is of far less concern than the actual thickness. However, with many in the electronics industry still referencing copper thickness in terms of weight, it is good to know how to convert. Memorizing the thickness of one-ounce copper can help a lot.

1oz Copper Thickness = 0.0014 Inches = 35.56 Microns (μm)

A sweet spot for copper pricing and availability is half-ounce (1oz divided by 2 = 0.0007 = 17.78 μm). Thinner-base copper allows for finer-pitch traces and more routes per layer. Thicker allows for higher current-carrying capacity at reduced trace widths. In general, it is easy to understand copper is sold by weight and therefore half-ounce copper should cost approximately half as much as one-ounce copper. This is mostly true, however, the issue to be aware of here is availability. The two most commonly stocked copper thicknesses in production shops are half-ounce and one-ounce. Designers must be aware deriving a cost factor for four-ounce copper by simply multiplying by 4X is missing an availability factor—production suppliers may have to special order copper outside of the standard thickness ranges. This could add lead time to a project costing much more than the copper itself in missed time-to-market and cost of lost sales.

**Therefore a \$2,
two-layer PCB will
cost an estimated
\$4 if the design
stack-up changes
to four layers.**



Cost of Adding Layers

Beginning with a single-layer design as a basis, most are surprised to find a single-layer and two-layer PCB cost approximately the same for materials and processing. This is because the cost-adder of lamination does not need to be included.

If it is determined the outer PCB surfaces will run out of space for routing, a decision to switch to a multi-layer design stack-up must be made. As a rule, layer pairs (two additional sheets of copper foil) are added. Perhaps one layer to serve as a ground plane and another layer to serve as a power plane. The average cost of adding a layer pair to create a four-layer PCB from a two-layer PCB is commonly estimated at double the price or a 100% cost adder. Therefore a \$2, two-layer PCB will cost an estimated \$4 if the design stack-up changes to four layers. The estimated cost of adding another layer pair to the design, increasing the layer count to six-layer, will increase the cost by another 50%.

Number of Layers	Cost
1-2	\$2
4 (add 100%)	\$4
6 (add 50%)	\$6

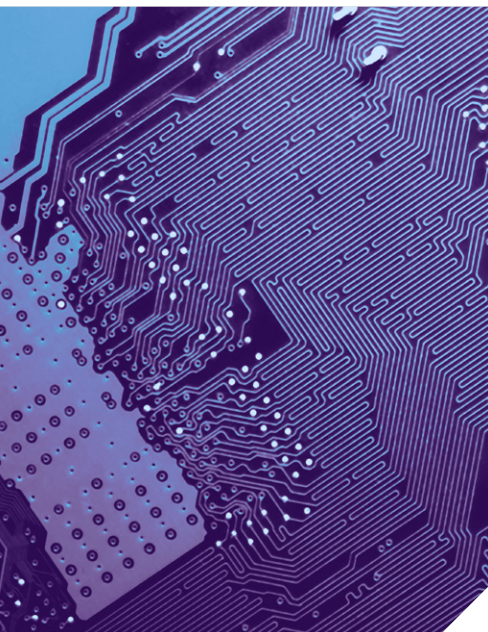
This rule of thumb can work as an estimation tool for adding additional layer pairs to a point, but when increased accuracy in targeting cost estimates for higher count multi-layer designs is required, it is best to obtain a quote from the PCB supplier who will be doing the work.

Cost of Shrinking Traces

To keep stack-up layer count low, shrinking etched copper geometry is an option. However, shrinking lines beyond the supplier's sweet spot can lead to cost-adders. To keep cost-adders low, it is important for designers to leave as much space as possible between densely routed traces for the supplier's print and etch processing. When the trace widths and spacing fall below the supplier's sweet spot, say .005 width with .006 spacing, the supplier may have to impose a 10% or more cost-adder to allow for extra material required to cover any scrapped PCBs. Again, if increased accuracy of cost estimates are required, contact the supplier.

Cost-Adders for Glass/Epoxy Material Types

One of the most common laminate material types used in the PCB industry is woven glass/epoxy, often referred to as "FR4." This material is supplied in many variable compositions and is available in many thicknesses with the most common supplied at .062 [1.57mm] thick. IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards is a good starting place for becoming familiar with FR4 laminates. There are many variables which can add cost, but the most common adder is for material with higher processing temperature ratings above 130° C.



A temp rating of 130°C attributed to the least expensive material may work well for a single-sided PCB design which will experience limited heat cycles or “thermal excursions” during processing. However, a multi-layer PCB with surface mount and thru-hole components on both sides will be subjected to multiple thermal excursions during processing. To keep the material from exceeding the material’s glass transition temperature (T_g), causing possible thru-hole barrel cracking and delamination, special additives are used to increase the material’s resistance to the effects of heat. Cost and availability for PCB laminates fluctuate greatly throughout the year. As always, if increased accuracy of cost estimates are required, contact the supplier.

PCB Stack-up DFM Considerations

Balancing the Stack-up

PCB warping can occur in a board when a designer is not aware of and/or does nothing to mitigate the mechanical stresses which can build up when laminating dissimilar layers of copper with various thickness combinations of glass-epoxy laminates.

It is important to make sure the materials on each side of the PCB stack-up centerline are matched. If the stack-up is laminated with disproportionate materials and material thicknesses, the unbalanced stack-up will experience warping due to built-in stresses incurred after heated lamination and cooling.

The balanced stack-up on the right shows symmetry of materials on each side of the PCB centerline, preventing warpage of the PCB after lamination.

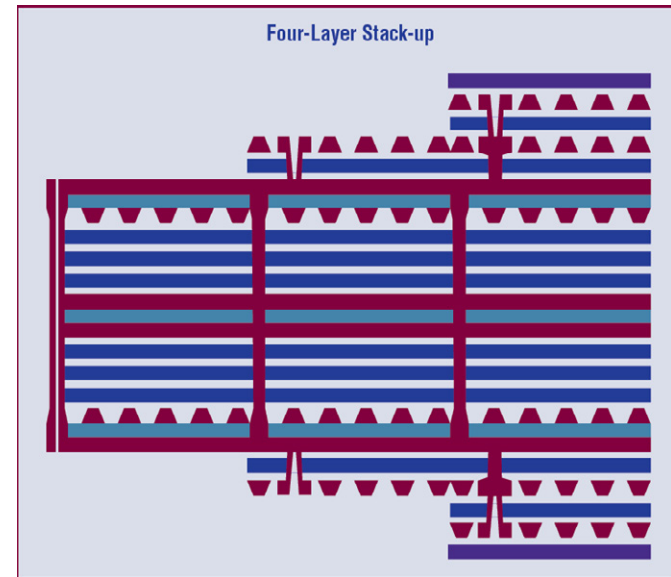
Core Construction

There are a few ways PCB suppliers accomplish building up a multi-layer PCB. One method is by employing core construction. Double-sided cores are printed and etched and then bonded together with a material called ‘prepreg’ or ‘B-stage’ material. Prepreg is basically the same type of glass-epoxy material used for the core, but it is not fully cured. It remains tacky as the board layers are stacked up in a press and then fully cures as heat and pressure are applied. Core construction in its simplest form is rarely utilized except on microwave PCBs where very expensive, high-tech microwave laminates are combined with low cost laminates to achieve a compromise solution for performance and price. This type of four (or more) layer stack-up is called a “core build.” It is made of core material on the outer layers.

The impedance must be achievable in manufacturing, based upon good stack-up design.

Foil Construction

The most common method used by fabricators for laminating multi-layer designs is the foil construction method combined with a sequential lamination process. In sequential lamination, cores may be individually printed, etched, and even drilled and plated prior to being laminated together with other cores. Individually selected sheets of copper and prepreg (or “B-stage”) laminate materials create a diverse combination of layer interconnects. These were formed during multiple press cycles of the multilayer manufacturing process. The foil construction methodology also has the advantage of “dialing in” distinctive combinations of glass-epoxy weaves which use unique resin-to-glass ratios, yielding exceptional dielectric properties to help control trace impedance as required.



Specifying Impedance

It is not enough to simply specify an impedance on PCB traces. The impedance must be achievable in manufacturing, based upon good stack-up design. The PCB fab shop is allowed three ways to adjust trace impedance accurately on a PCB once the designer has done his or her part by using a simple impedance calculator to get close. When designers select trace widths based upon values determined by an impedance calculator, the manufacturing team can easily adjust the dielectric strength and thickness of the prepreg materials in stock. The different prepreg materials can be used to adjust the trace distance from the reference plane to achieve the specified impedance value. If necessary, they can even adjust the trace width slightly in the CAM department to dial the design right in. However, it's important to

remember the PCB fabricator can only achieve impedance in this way if it is noted on the PCB fabrication drawing. The note must state that the three specific characteristics may be varied.

Impedance-controlled designs allow adjustment of three physical variables in the stack-up:

- Dielectric and value of the material (ϵ_r)
- Trace distance from reference plane(s)
- Trace width and spacing

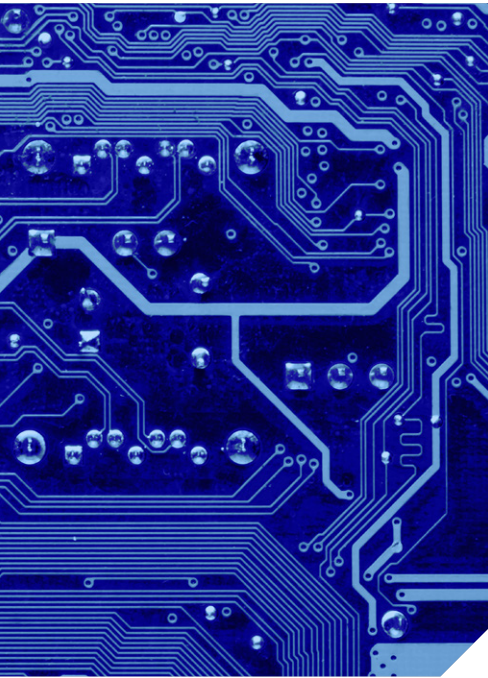
There are sometimes specialized customer engineering requirements which will not tolerate variations in physical composition or structure. Hybrid material-controlled stack-up specification is less common and usually specified when PCBs will be required to fly into space or be utilized in very specialized circumstances. This methodology is very expensive and results in long lead times due to the need to procure specialized materials and processes. If material-controlled stack-up methodology is not required for performance, it must be eliminated from the design process as it will mostly yield higher-cost parts or a no-bid on a request for quote.

Trace width vs Copper Thickness

Sometimes making the decision to add layer pairs to a PCB stack-up is based upon a designer running out of routing space. As an example, if the trace routing width was originally estimated to be .010 with .010 spacing with copper weight at 2oz (.0028 thick) for current-carrying capacity reasons, but won't fit, what can be done to get the trace routing to fit and how will it affect the stack-up?

One way to handle this would be to examine whether shrinking the trace widths and spacing would allow all the routing to fit. If it is determined the routing would fit if the traces and spacing were reduced to .006 with .008 spacing, why not? Is there anything else to consider? Not so fast.

This means as the trace-width is reduced, the height of the trace must shrink proportionally along with it.



By checking in with the PCB fabrication stakeholder (as Ian in our story forgot to do), the prudent designer will find the print-and-etch factors for trace widths must stay proportionate to each other to some extent. This means as the trace-width is reduced, the height (or thickness) of the trace must shrink proportionally along with it. This will indeed need to be reflected in the PCB stack-up detail. Due to the nature of the PCB printing and etching processes, the acids attack the sides of the traces in contact with the substrate material more aggressively causing a trapezoidal effect. If the copper thickness is not reduced, the width of the copper at the base may become too narrow and fail:

Balanced Etching Between Layers

Besides etching considerations for trace routing, imbalanced etching of larger copper areas of the PCB can contribute to layer stress and warpage too. PCB layers which are etched leaving heavy and lite portions of imaging cause an automatic balancing challenge for the PCB fabricator.

Commonly, PCB core laminates are supplied with copper foil laminated evenly to both sides. The laminated copper expands and contracts at a much different rate than the glass-epoxy laminates, but when the copper exists on both sides of the glass-epoxy equally, the stresses are evened out, allowing the core to remain flat. However, a challenge is introduced when a large percentage of the copper is only etched off one-side of the core.

If there are dense copper patterns on one side, try including copper 'fill flooding,' by using ground fills on the opposite side to balance out the copper on each side.

However, in the case of multi-layer PCB stack-ups, it is usually bad practice to randomly flood every layer with copper flooding for the cause of balancing the stack. In general, every signal layer deserves a solid return path laminated adjacently to it in the stack-up for signal integrity purposes.

PCB flatness is achieved by design. While it would be easy for the PCB fabrication engineers to mechanically warp the boards in the opposite direction to meet any flatness specifications for problem designs, it would also be very unethical. It is a simple fact that upon experiencing heat in the wave solder or reflow oven, an unbalanced PCB will again warp to its unconstrained equilibrium, and the problem will be exposed. Therefore, fabrication engineers appreciate a designer who is concerned about properly balancing the copper in the design stack-up during layout. It is the best preventative method to achieve PCB flatness.

Stack-up Best Practices:

- ☐ Always provide a closely-spaced, adjacent, solid plane return path for signal traces to reduce EMI.
- ☐ Alternate signal and plane layers symmetrically about the centerline of the PCB to create a balanced stack-up.
- ☐ Use an impedance calculator to determine general widths for impedance control. There are many free impedance calculators available on-line which can serve this purpose. The designer's job is to get close, so the fab shop can then dial it in.
- ☐ Allow the PCB fabricator to adjust trace width, dielectric thickness (distance to reference plane), and dielectric strength to achieve specified impedance. Do not specify physical material dielectric properties of a PCB stack-up unless absolutely required to do so.
- ☐ Never allow the fabricator to adjust the copper thickness to control impedance. It is ineffective and if adjusted thinner, may devalue required current-carrying capacity of conductors; decreasing performance.

Chapter 8

Routing and Planes

Now that we have established the PCB stack-up is more than just a thickness diagram, we have laid a foundation for routing and utilization of copper planes within the layout. Layout is usually thought of as merely a job of “connecting the dots” by those who do not understand the complexities of PCB design. This perception is true to a very small extent, but PCB layout is far from simple. After routing and completion of the layout, when the PCB goes on to be manufactured and assembled, the dots which a PCB designer has connected will have turned into copper connections which must carry electrons. The copper and its surrounding substrates must be properly configured to be manufactured and assembled together with a myriad of components which must operate by using those electrons. There are thousands of things which can go wrong.

In Ian’s design in chapters one and two, the auto-router routed two-hundred and fifty-six nodes of ground connections using 3 mil trace widths. This simply never would have worked—Ian’s circuitry needed solid power planes to provide power and enhance performance. Ian allowed the software defaults to have their way with his design which proved very costly for all project stakeholders from a time and expense standpoint.

Even if Ian’s design had made it all the way through the manufacturing processes, the electronic circuitry within the board would not have performed as intended. Without knowledge of key design fundamentals, relying on automated features (like the auto-router in default settings) can cause a serious design wreck. Left to its own devices, an auto-router may pack all the signals together, causing a great degree of cross-talk, destroying their ability to perform

There are five important topics to consider during completion of the layout:

PCB Layout
Design Rules
Defining Vias
Utilizing Planes & Pours
Impedance Control & SI
Routing

Design Rules

To successfully complete a PCB layout, it is very important to set the design rules to match the estimated producibility class of the design. PCB design rules can be set in most layout tools which allow generic settings to be saved. Design Rules Checking (DRC) tools will check against these rules in real-time, providing you feedback as you go. Having this real-time feedback is invaluable as a designer. Trying to keep track of all the rules and how they interrelate manually is not a task you want to take on.

Just about everything pertaining to copper in a PCB design is controllable in the design rules portion of a PCB layout tool. The pre-set design rule values or “default settings” are set by a layout tool provider who knows nothing about the new layout a designer may be working on. There can be hundreds, if not thousands, of control variants in the tool’s default settings which can cause catastrophic manufacturing conflicts if not re-set to match the requirements of a new project.

Once the connectivity of the layout is synchronized with the schematic, it is essential for a designer to surmise which general design rule constraints will best control the new design and reset them for the required result.

For instance, if not re-set, a pre-set copper plane clearance value of .005 [0.127mm] will yield an un-manufacturable etching condition if a 2oz base copper thickness requirement has been setup in the stack-up. When the thickness of copper used in a stack-up is increased, the copper clearances must be increased accordingly. Unfortunately, PCB software does not check for this condition, but it will adjust for the condition. The PCB design engineer must control the copper clearance setting to ensure there will be enough artwork clearance for the supplier to etch enough copper clearance.

Another negative result of failing to reset default values might involve noisy clock lines. If a clock line is not identified as an aggressor and is treated with the same 5mil default spacing constraint rules as other lines, there is a risk of the line being packed too closely to other lines during routing. To prevent this, a designer can specify special spacing constraints for aggressive or sensitive lines and add them to a design “class.” A design constraint class may be assigned many unique design attributes, including wider spacing constraints. If the class spacing is set to 20mils, adding a clock line into the class will impose the new spacing of 20mils onto the line and the design rules checking process will audit for the condition. In general, there are five basic areas which will need to be configured to match the design you are working on. Four of the five category settings directly affect manufacturability: copper plane clearance, part outline clearance, drill (hole) clearance, legend (markings) clearance, and trace length clearance.

The last setting category affects performance: trace length and clearance. It will likely take some time for a new designer to learn how to control all the design rule settings. However, concentrating on these five categories first should help.

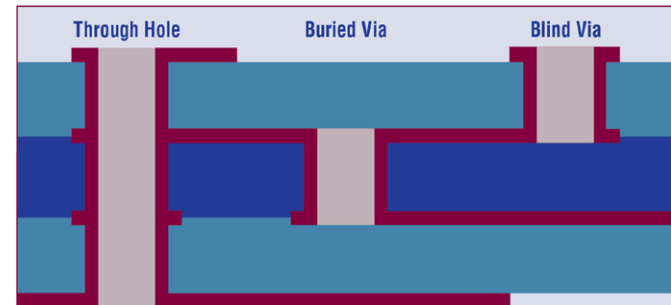
Saving PCB design templates for various types of designs can save a lot of setup time at the start of a design.

Additionally, it is always a good idea to check in with the appropriate manufacturing process stakeholder when initially setting these values. For best DFM, never set values to the stakeholder's minimum or maximum capability. Design rules in a PCB layout tool can be a blessing if understood and set properly. However, they can also be a curse if not carefully considered and reset from the default settings.

As an alternative to readjusting the preset design values in a new PCB layout database each time a new design is started, PCB design engineers often create their own PCB layout templates. A personal PCB design template can be easily established by making all the desired settings such as color preferences, DRC settings, via size, layer stack-up, formats, and title blocks to a generic design database and filing it as a design template. Saving PCB design templates for various types of designs can save a lot of setup time at the start of a design. Design templates may be created for layer count for 2, 4, 6 (& more) layer rigid designs or for special types of designs, such as flexible circuits or boards with standard card edge connectors.

Defining Vias

Via size requirements need to be considered at the beginning of a layout. Vias are small holes in the PCB which are plated to make interstitial connections to multiple circuit layers. In other words, making connections from one side of the board to the other or to inner layers requires a via. There are three general types of mechanically-drilled vias: through-hole, buried, and blind.

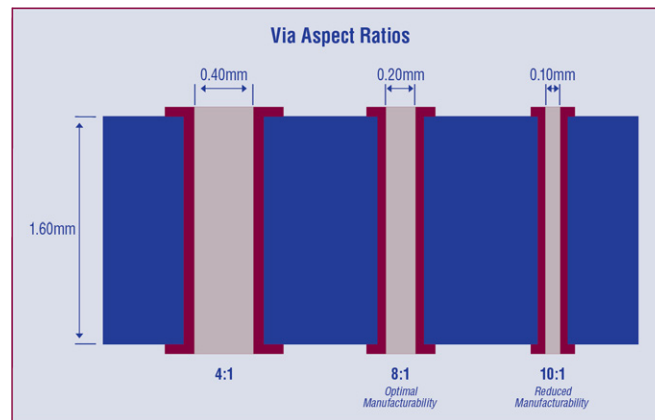


Vias require a pad etched in copper on each layer which will be electrically connected. The pad diameter needs to be small enough to not eat up valuable routing area; however, the pad diameter must be large enough to accommodate a hole-forming operation such as drilling or laser-forming.

Drilled Vias

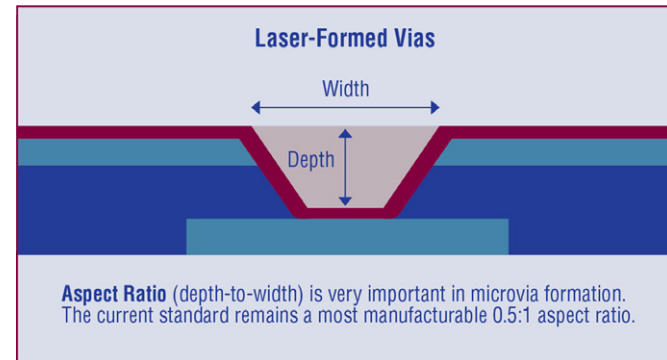
Mechanically-drilled via holes are kept small for space concerns and have a special relationship with PCB thickness due to the process by which the holes are plated. For the walls of the via to form a plated through-hole (PTH), a very fine solution of copper (referred to as CuPosit) must thoroughly coat the surface of the holes. CuPosit forms a micro-layer of copper on the bare wall of the drilled hole. The process requires the CuPosit to wash freely through the holes to coat the entire surface. However, this process is impeded when the hole diameter is too small in relationship to the thickness of the PCB material it goes through. In the PCB manufacturing world, this relationship is known as the aspect ratio of the PCB.

If the smallest hole drilled through a .063 [1.60mm] thick PCB has a diameter of .008 [0.20mm], the PCB is determined to have an aspect ratio of 8:1. ($.063/.008 = 8$). Therefore, if the smallest hole drilled through a .063 [1.60mm] thick PCB has a diameter of .006 [0.15mm], the PCB is determined to have an aspect ratio of 10:1. ($.063/.006 = 10$).



Laser-formed Vias

The concept of aspect ratio plays a part in the formation of laser-form holes in PCBs as well. Due to the conical shape of a hole formed by the laser while burning through material, designers must pay very close attention to the width / depth relationship capabilities of the process. A 1:2 ratio between the width and depth is considered manufacturable.



How a common “10/20” Via is derived

Hole diameter tolerancing for vias is usually expressed in a bi-lateral form. Example $\pm .003$ [0.08mm]. This is an important concept when configuring a via because of the relationship of the hole to the pads. This relationship will form a supporting copper ring called the annular ring. Once a via hole size is selected, a padstack can be designed to make certain there will be an annular ring supporting the hole and the worst-case tolerance condition of the drilled hole. If we were to start with a hole specification of $.010 \pm .003$ and want to determine an optimal pad diameter, we would need to start with the maximum allowable size of the hole. In this case, since the tolerance is $\pm .003$ we would add .003 to the nominal hole diameter of .010 to reach .013. PCB manufacturers need to oversize the hole to allow for plating by approximately .002 so this value needs to be added. It is also good practice to allow a couple more thousandths-of-an-inch to allow for locational tolerances.

After adding these factors together, we have derived the maximum hole consideration and can add a minimum copper ring around it to derive the pad diameter. Here's how it looks:

.010 nominal hole value

.003 added tolerance

.002 drilling oversize to allow for plating

.002 diameter positional tolerance to allow for hole alignment to pad

= .017 diameter max hole value

+ .003 minim annular ring allowance

= .020 minimum pad diameter.

This is a simplified explanation of a common minimum via/pad derivation. However, why design to minimum unless you must? Any PCB manufacturing stakeholder will appreciate another few thousandths increase in pad diameter to increase DFM, if you can afford the space to allow it.

Selecting the right type of via

Designers will typically create several via types within a layout tool's library for access during most any layout condition. A wide array of via selections make routing simple because the via "padstacks" are ready to be used dynamically without having to stop, create, check, and adjust. However, the new designer must realize the various vias are not to be inserted randomly—there must be good design reasons for decreasing size or increasing complexity of a via.

Selecting the proper via type will not only help complete trace routing, but can also help in alternate applications for uses like EMI shielding and thermal management. However, choosing any via type other than a common thru-hole via with a modest hole diameter/board thickness aspect ratio will most certainly incur a cost adder as well.

As with most things in the PCB manufacturing industry, as via size shrinks or the complexity goes up, the "yield" of the PCB run may go down as some part features, such as vias, fail to pass inspection. Scrap is the term used for parts which must be thrown out or recycled due to this condition. Knowing yield will go down due a design's complexity; the supplier will have no choice but to start a build with more material to make up the difference to be able to ship the required number of parts. This extra material and processing will be added into the price of the PCB run.

Blind vias will incur a cost adder because of a unique process involved which utilizes a controlled-depth drilling operation to connect an outer layer contact to an inner layer contact. After the controlled-depth hole is made, an additional plating operation is required to make the connection by plating the newly created hole walls between the top an inner layer pad surfaces.

Power planes are the most effective way to distribute power to almost every part of the PCB.

Buried vias will most certainly incur even a higher cost. Buried vias require a drilling and plating operation between copper layers separated by core material which will end up as an inner layer pair of a PCB. Once the layers are printed, plated and etched, the layer pair may be laminated together with more pairs and sandwiched between outer layers of more laminate materials.

This method of sequential lamination “buries” the thru-hole vias of the inner layer pairs with prepreg material.

A great benefit of using this type of via strategy is it allows the areas above and below the buried via to be utilized for additional routing on very dense designs. Buried via technology comes with a high cost adder though, as multiple boards are required to be processed separately and then laminated together into a single PCB.

Vias are often a necessity in the design. Knowing the different types, benefits, and potential costs will help you make sure you select the best via for your needs avoiding cost and manufacturability issues downstream.

Utilizing Planes and Pours

Power planes are the most effective way to distribute power to almost every part of the PCB. Power planes are simply formed by adding layers of copper foil to the stack-up and connecting them to power or ground. Smaller surface mount technology (SMT) parts located any place on the board surfaces can connect to a plane by use of a via. Larger SMT parts requiring more power can use multiple vias connected to the power planes. By their physical nature, thru-hole parts will easily connect

to the planes as required. However, for high-current requirements, designers sometimes add support vias around a component pin to increase the current path to the pin.

The thickness selected for copper planes is variable, but most designs make use of readily available thicknesses such as .5oz or 1oz. For higher power requirements, heavy copper foil is available in 3oz and greater thickness. Designers must keep in mind however, there are tradeoffs in choosing copper thickness regarding current capabilities vs etch-ability. Thinner copper foils are suitable for printing higher-detailed patterns and can tolerate less clearance between features, but at a cost of requiring wider areas of uninterrupted copper across the board area. When using copper over 1oz, keep in very close contact with the print and etch capabilities of the supplier to make sure adequate copper clearances are maintained.

Split Planes

Very often, circuit layouts cannot be accomplished without splitting power into several potentials which will benefit from forming wide swaths of copper to reach designated areas. However, dividing a plane layer into several portions forms islands separated from the main plane by splits. Due to these splits creating the potential adverse EMI conditions discussed later in this chapter, routing on layers directly above or below these split areas should be avoided.

Besides power distribution, Copper planes can be utilized for many other purposes such as:

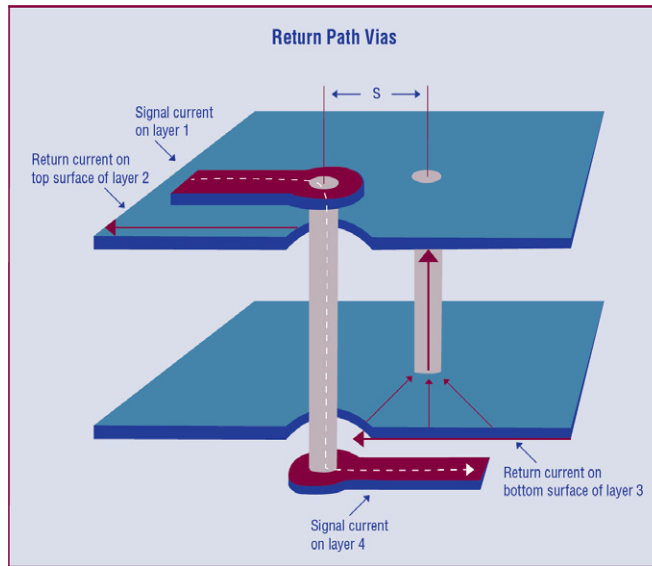
- EMI reduction return path
- Added capacitance
- EMI shielding and ESD guard band support
- Thermal management – heat sinking

EMI Reduction Return Path

To keep unwanted electromagnetic interference (EMI) to a minimum, providing a solid ground plane beneath traces has been proven to be the best solution. When crossing the routing surface of a PCB, a current running through a trace will always seek to close its circuit by returning to ground. Providing a ground plane beneath the conductors will provide the shortest path. It is important to remember DC current running through a trace will always take a path of least resistance while AC currents will take the path of least inductance.

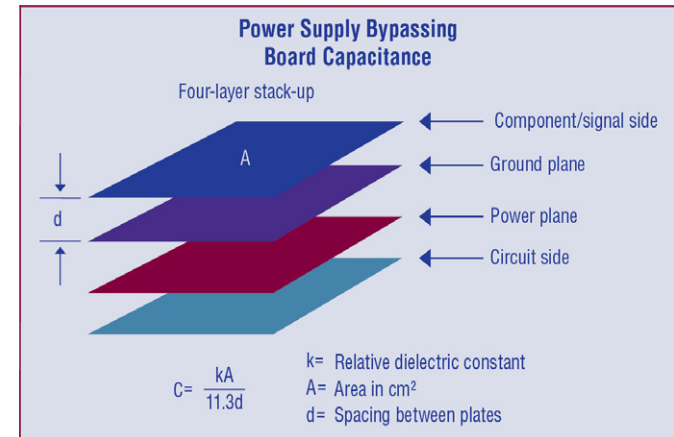
Creating wide conductor paths are helpful in keeping EMI to a minimum. Any current that returns through the ground plane, flows close to the forward current path. This minimizes loop inductance, thus minimizing generated interference and received susceptibility to interference.

Analog and digital circuitry must be kept separate whenever possible. Fast-rising edge rates create current spikes flowing in the ground plane. These fast-current spikes create noise which can corrupt analog signal performance. Analog and digital grounds are normally tied at a common point, sometimes referred to as a “bond” or “ground bond” point to minimize digital and analog ground currents and noise. Without going into a lot of physics, this is what happens when you use ground planes—EMI problems are instantly reduced by a large factor.



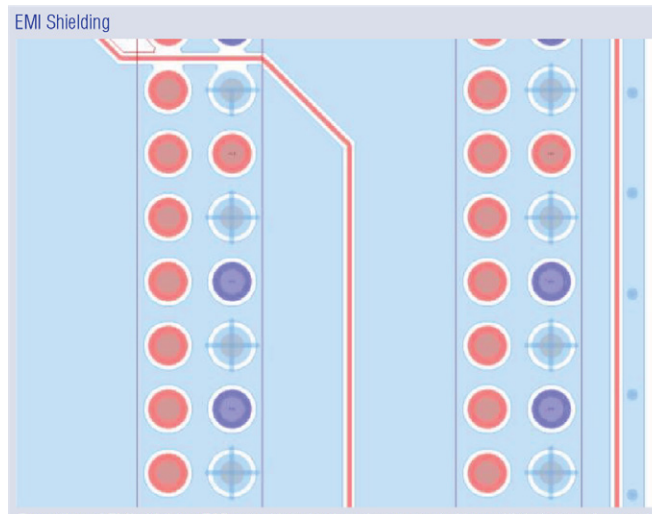
Added Capacitance

Power and ground planes are often utilized for high-frequency bypassing along with conventional capacitors. Placing power and ground planes closely together in the stack-up, separated by only a thin layer of dielectric material turns the planes into an excellent high-frequency capacitor. The added inter-plane capacitance provided by closely placed power and ground plane layers can help to reduce effects of EMI.



EMI shielding and ESD guard band

A layer of copper attached to ground can serve a dual purpose of providing ground where it is needed, while simultaneously being used as a shielding layer between sensitive and aggressor traces, if the traces are routed on separate layers with the ground plane between them. Often, multiple ground-plane layers can be stitched together to form a type of faraday cage which can be utilized to keep EMI energy in or out. A variation of this technique can also be employed to direct the flow of any electro-static energy that would meet the PCB. An ESD ring formed around the PCB can be an inexpensive additional safeguard to prevent ESD from reaching critical circuits.



Planes as a Heat Sink

A side benefit of solid power planes is they are very good thermal conductors. If a high-power component is mounted so its body is in contact with an outer-layer copper plane, the plane will naturally draw heat away from the component through the process of conduction. As the heat moves through the copper plane, it spreads out and dissipates into the air through the process of convection. If more dissipation is required for a hotter component, multiple planes may be “stitched” together from layer-to-layer using vias. These “thermal vias” assist in drawing heat away from one side of the PCB and distribute it more effectively to inner and opposite sides of the PCB for dissipation.

A long time ago, creation and use of power planes would be covered in a section like this with a simple picture of a geometric blob of etched copper and it would make reference to its similarities to “flat wire” for distributing power to multiple points on a PCB. We’ve seen here many ways in which copper foil helps distribute power, how etched and embedded copper foil can be utilized for EMI reduction as a return path, and how multiple layers of ground and power can be laminated closely to increase capacitance and even be utilized in thermal management applications as a thermally conductive or convective heat path. A cool thing about a PCB design layer is it starts out as a solid plane. Carving away just a little to form a multi-purpose thermo-electro plane shape seems only limited by one’s imagination.

Impedance Control and Signal Integrity

Industries requiring quick digital applications such as telecommunications, video, computing, and others rely on impedance control in design to help minimize signal degradation and improve signal integrity. A PCB design engineer needs to recognize controlled impedance requirements on a schematic and be able to manipulate several parts of the design layout to achieve the requirements.

Controlled Impedance

Impedance control on a PCB is required when performance dictates signal degradation in a circuit cannot vary beyond a specified amount expressed in ohms. Impedance control requirements for PCB layout can be addressed physically in the layout by identifying which nets in the design are to be controlled by their specific impedance value. Effectively design for controlled impedance within any specific layer through the use of a simple impedance calculator. By experimenting with values, you can adjust the PCB traces and stack-up. Remember, it is a designer's job to get close, but it is the fabricator's job to dial it in. Always seek approval from the PCB fabricator after estimating impedance stack-up solutions. Make sure to leave enough room for the supplier to adjust the trace width, dielectric thickness (distance from trace to plane), and dielectric constant value. It is wise to not allow the supplier to make any adjustments to copper thickness as it can affect current-carrying capacity of power traces residing on the same layer.

Impedance Calculator

Conductor Impedance

Conductor Width (W)
 mils

Conductor Height (H)
 mils

Frequency (MHz)

Note:
This calculator uses a complex formula, not the simplified formula. Results track the Sonnet 3D solver.

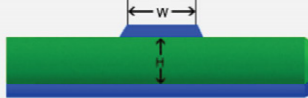
Er Effective = 3.0856

Zo

Lo

Co

Tpd



**Note: This calculator can be found on satumpcb.com*

It is up to the designer to calculate the design options for the line width and spacing based upon manufacturability.

Signal Integrity

Certain circuits require routing parameters which must be held for the device signals to run properly. Signal routing parameters are documented in the component manufacturer's data sheet. There are several parameters to be aware of when performing placement of the chip, its related components, and when completing the routing. These include:

- Lengths and routing order of critical signals which must be matched to related signals
- Hub routing constraints where a signal routes to a given point and then splits off to several length-matched destinations
- Distance to adjacent signals could allow for unwanted signal coupling or “cross-talk”
- Impedance control, either single-ended or differential
- Unbroken reference plane running beneath signal routing layers

Pro-Tip from Mike Brown

“The PCB designer has to consider inputs from the electrical and mechanical sides and turn it into design that will satisfy fabrication and assembly. The EE will have a set of goals and the ME will have a different set of goals. It needs to be understood that in PCB layout, there are certain checkpoints which must be passed along the way. The designer's responsibility is to sort through all of the information from these competing disciplines and make sure that all of the checkpoints from each side are met.”

Sometimes PCB electrical performance considerations conflict with manufacturing considerations. A designer must be able to quickly assess the appropriate compromise between the two. For instance, a design may call for a differential signal impedance, requiring a certain spacing between two signal tracks routed at a specific width. It is up to the designer to calculate the design options for the line width and spacing based upon manufacturability. This is essential to achieve a solution to match the overall manufacturing class of the PCB. Sometimes the routing width for some critical nets may have to be routed using a special calculated width. It is best to try to calculate a width close to most of the routing widths on the specific layer. However, if it turns out it can be routed at the same width, adjusting the width value by a small amount—say 7.1 mils from 7 mils—will help the supplier's CAM department find the net to be controlled easily without having an impact on impedance.

Often companies will have an SI expert or consultant who specializes in these types of high-speed signals to ensure proper operation. While every designer may not be an SI guru, having a solid understanding of the critical signals and the general requirements needed to ensure acceptable signal integrity will help keep any issues found by your SI expert or in test to a minimum.

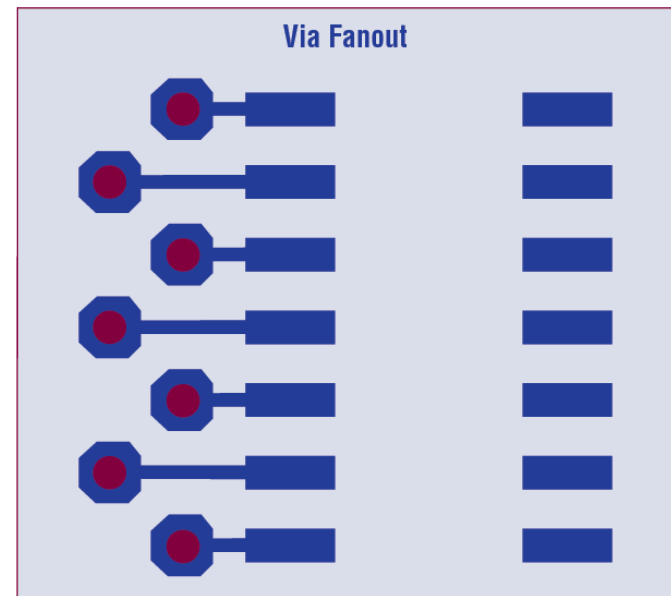
Routing

PCB routing is a highly subjective topic due to the myriad of various constraints which may be present within the PCB design. A designer must not only get a PCB layout routed, but the PCB design must perform. Subjectivity aside, there are a few considerations which must be implemented in the interest of both electrical performance and DFM. These include:

- Fanout
- Routing Power
- Routing Critical Lines

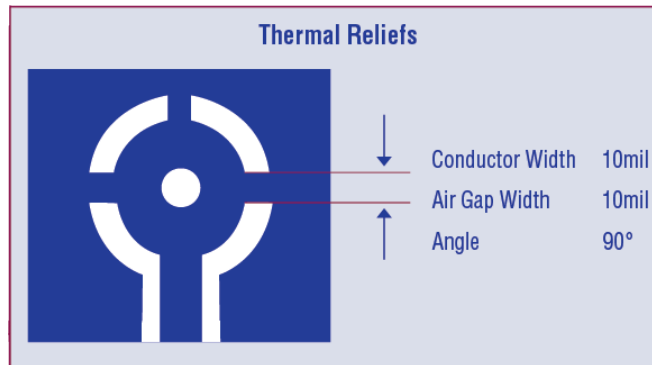
Fanout

It is common practice to perform a fanout of via connections from each connected part land. A fanout pattern helps to take groups of traces which are designated for inner-layer routing to an organized pattern of vias for optimized routing. This operation can be performed manually or automatically. Remember, this is based upon design tool settings and should not be performed without consideration of the impact the via fanout can have on routing. Like many operations in design layout, the best methods are often performed in an iterative fashion. In the case of via fanout, it is perhaps best to perform a fanout of the power and ground pins first, optimizing and then locking them into place, before moving on to fanout of critical signals and followed by everything else.



Routing Power

The most common method of connecting a component pin to a power plane is with a trace. For anyone out of school who has been exposed to electronics theory via ohm's law, the simple solution to avoiding the effects of voltage drop, inductance, and restrictions in current flow while routing power pins is to make the trace as short and as wide as possible. While this could be considered a good rule of thumb and keep a designer out of trouble electrically, a designer must not forget how this rule of thumb may affect DFM.



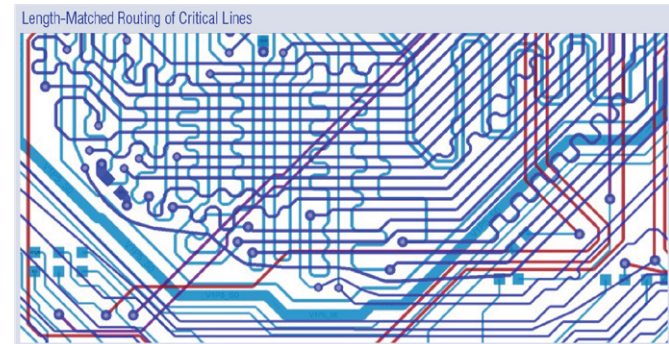
When attaching robust amounts of copper to a component pin to improve electrical conductivity of the current path, a designer must remember copper is also a good conductor of heat and is often used for heat sinking. Therefore, it is possible to add so much copper to a component pin that the heat applied during a soldering operation will be conducted away from the component pin, preventing the pin from soldering properly. This condition is referred to as a cold solder joint and can be prevented by spreading the connectivity of the copper over multiple layers to provide thermal relief. For instance, if it is determined that connecting a small pin to a .050 wide conductor is required for electronic performance, the conductor may be split into several, separate widths and dispersed throughout the layers of the PCB to provide better thermal relief for soldering.

Using industry guidelines such as IPC-2221 is a great resource to help you make sure you are meeting current carrying capacity requirements during power line routing.

Routing Critical Lines

Routing the most critical lines is the next step in the process. Often referred to as “the criticals,” these nets require special attention due to constraints which may be associated with their capacity to perform based upon design rule factors.

Line functionality, such as clock or power-switching lines, can be considered aggressor lines. They can create noise—very much like the type of noise an AM car radio puts out when driving under power lines—which can be detrimental to nearby data traces. Special clearances must be considered based upon many physical characteristics of the layout. Basic clearance calculation requires using front-end analysis tools to mitigate any problems. The clearance values, along with many other constraint values, may be added to the schematic. These constraints may then be passed along into the layout for consideration and final checking.

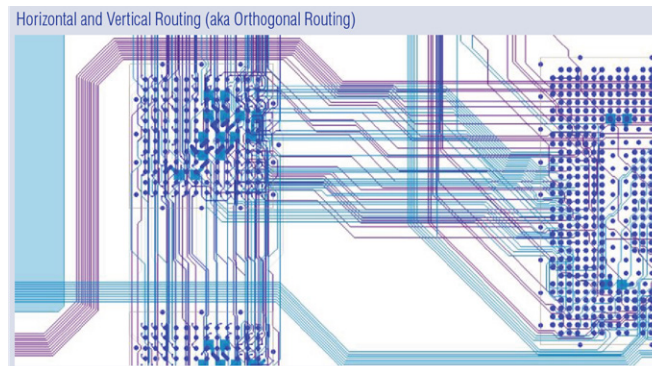


A trace is a transmission line and will always seek the shortest return path.

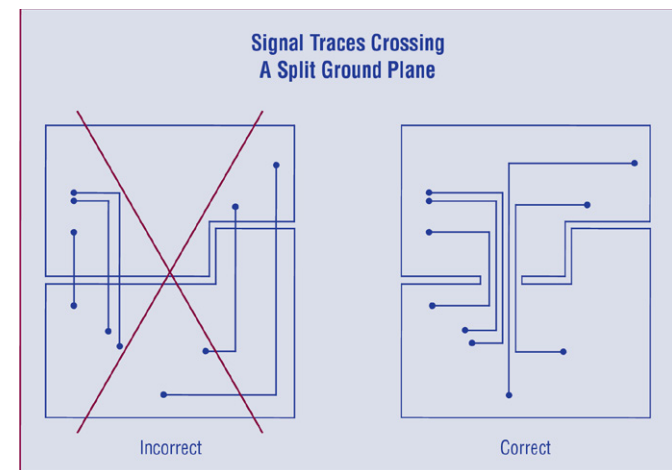
Routing a simple net adds a copper trace between two points on a PCB layout. However, routing a complex net often requires routing lines between many “nodes” in the circuit. Like carving a road between several mountain ranges, avoiding lakes and any private land. Careful thought must be put into the best routing path for a critical signal trace. Deciding to change layers using a via or taking a longer path to complete the routed net on a single layer are decisions which can potentially affect the performance of the signal.

Signal routing should start after all the plane layers and critical routes are defined. When trying to decipher which layers are the best to route on for electrical performance, it is important to understand ‘best’ is a relative term. It is determined by the ability to design a connection which will achieve a specified performance requirement on a trace without adversely affecting functionality or cost.

In general, biasing entire routing layers in a horizontal or vertical direction is considered the best use of available real estate. Adjacent layers can be alternated so distance can be increased between layers with traces running in the same direction, preventing coupling with critical lines.



While considering critical route paths, double-check the adjacent layers for any lines running in parallel. Some layout tools provide automated checks for this condition. If available, learn to utilize this capability to its fullest.



It is important to avoid crossing splits in adjacent (underlying) plane layers. A trace is a transmission line and will always seek the shortest return path. A plane running a few mils underneath signal traces provides an excellent return path for a signal. However, if the plane has a gap which the trace runs across, EMI—commonly referred to as noise—is generated and can become problematic for surrounding circuitry. Some CAD design tools will check this for this condition, so investigate and learn the proper DRC settings to leverage this capability to its fullest.

Always review the route path for each net to make sure it has been run as efficiently as possible. A net analyzer is included as a feature in most layout tools and can help. Circuitous routing paths or routing paths which double-back on themselves are a scourge to efficient use of routing area and can have negative effects on performance. A net analyzer can list and sort nets within the design by length and highlight each route path individually starting with the longest first. A net analyzer is an effective tool for catching wayward critical route paths, so they can be shortened.

Routing common traces between components using modern PCB tools goes quickly and can be quite fun. It can be tempting to get going on the “easy” routing before firmly establishing the routing and locking critical routes first. There is a saying in the PCB design industry: “90% of the routing on a PCB takes only 10% of the time, while 10% of the remaining routing can take 90% of the time.” This perspective describes a designer’s experience toward the completion of a layout when the fun of routing turns over to an ever-increasing challenge. Suddenly there is a realization all the fun routes have eaten up all the routing space. The routing challenge will most certainly turn into defeat and a complete do-over if the remaining 10% of the routing (mentioned in the saying) includes any critical signals. Keep routing fun and challenging—consider critical net noise, clearance, and establishing shortest routing paths first. At the same time, consider avoiding adjacent layer parallelism and eliminating circuitous routing paths. Avoid complete routing do-overs by routing critical lines first.

Conclusion

It might be easy for those who do not understand PCB layout to sum up the process as simply “fitting the parts on the board and hooking them together.” The intent of this chapter has been to give a new designer some basic routing points to consider before, or instead of, simply activating an auto-routing routine.

Successful routing and plane utilization has a direct effect on circuit performance. Implementing set-up, routing and establishing copper planes in a PCB layout can really make the difference between a dot-to-dot hook-up technician and a designer. Metaphorically, this comparison may be likened to the steps a skilled photographer would implement to create a classic photograph. Without understanding how to properly setup and manipulate the subject matter, lighting, and exposure controls, a camera operated by the click of novice may only yield a cheesy snapshot.

Tips for Routing and Utilizing Planes:

- ☐ Become very familiar with the design rules setup for your layout software. Understand how routing can be controlled or constrained to route based upon rules defined and imported from the schematic or set them manually before routing begins.
- ☐ Set spacing constraints for individual lines and traces, not only for fabrication processing, but for electrical performance.
- ☐ Create design templates to save time.

- 
- ☐ Nets can be grouped into classes for organizational purposes. Assign trace width values to all nets.
 - ☐ Select a via size based upon estimated design density to allow the largest, practical via pad diameter. Always speak with the PCB supplier to verify the via-to-pad diameter ratio allows enough annular ring to over-drill prior to plating.
 - ☐ Via size and technology requirements need to be considered at the beginning of a layout. Make sure the aspect ratio of via-diameter-to-PCB-thickness is manufacturable. Allow enough pad diameter to form a sufficient annular ring around the drilled hole. Consider the supplier's achievable aspect ratio of PCB thickness-to-via-size when defining vias.
 - ☐ On multi-layer designs, perform a via fanout operation manually or automatically to reserve multi-layer interconnection points for each pin prior to routing. Audit for via size, placement, and test point assignability.
 - ☐ Utilize solid copper layers to form power planes which can also be utilized for EMI shielding and heat sinking.
 - ☐ Use copper pouring to widen connectivity in smaller, localized circuit areas to increase current-carrying capacity and lower inductance.
 - ☐ Route remaining power connections after establishing part placement and power plane definition. Base power line width upon copper thickness and proven current-carrying capacity calculations in IPC-2221.
 - ☐ Select routing line sizes which can be easily manufactured by the supplier.
 - ☐ Route all critical signals to establish the shortest path with the fewest possible vias while maintaining adjacent proximity to a solid plane return path.
 - ☐ Consider impedance requirements during setup and adjust line widths based upon calculations from a simple impedance calculator. Remember, the designer's job is just to get close. The PCB supplier will dial in the impedance by adjusting three variables if you allow them to: Trace width, dielectric constant of the material, and distance of trace to reference plane.
 - ☐ 'Freeze' or 'lock' the critical nets so they will not be affected by push & shove routines as the remainder of the routing is completed.
 - ☐ Follow a routing order which allows via fanout first, routing of power second, and attention to remaining signal routing third.
 - ☐ Review routing to check for circuitous route paths which may be optimized. Always check for signal lines crossing splits from an adjacent power plane and mitigate.
 - ☐ Once routing is complete, perform signal integrity checks and adjust as required.

Chapter 9

Fabrication Data & Documentation

CAD/CAM data has taken over the world of electronics. Since design and manufacturing is driven by data, much of what is accomplished on the PCB fabrication PCBA manufacturing floors has been standardized. Gone are the days of tape and mylar layouts in which designers served as artists, manually creating large-scale PCB artwork which would have to be photographically reduced to be used as a “photo-tool” to define the image of the etched copper PCB layer. And gone are the days of drill master artwork which would be used to manually “bomb-site” and program a PCB drill tape.

However, the electronic manufacturing service provider's challenge has not only been to create the machinery and processing to manufacture new PCBs and PCBAs using data, but also to keep up with installing the new generation processors which are running at incredible speeds and require special considerations which cannot be defined using data alone. Along with the ‘traditional’ CAD/CAM data, there is still a need for textual information in the form of notes and special detailing to provide a complete engineering design package and help ensure a smooth manufacturing process

Pro-TipFrom Mark Thompson

“We love it when designers call us with new technology questions. Good designers will admit they don’t know what they don’t know – and they won’t know until they ask. Fabricators need to know up front if an EE has special material requirements, especially if the EE has their mind on a specific dielectric or material to be used in the design, as availability buildup strategy is an issue here.”

You have spent a lot of time designing your board and getting it ‘just right’. It is critical you provide your manufacturing partner the information they need to ensure they can build your board to meet your design intent. Without guidance from you, the designer, the fabricator will either be forced to make assumptions or delay manufacture while they seek to ask you questions they don’t have the answers for.

Let us look what composes a complete PCB data package and examine the notation and graphic documentation which must accompany it.

Fabrication Data
File Naming Convention
Gerber Data Files
Design Continuity Verification File
Drill File
Neutral Database File

File Naming Convention

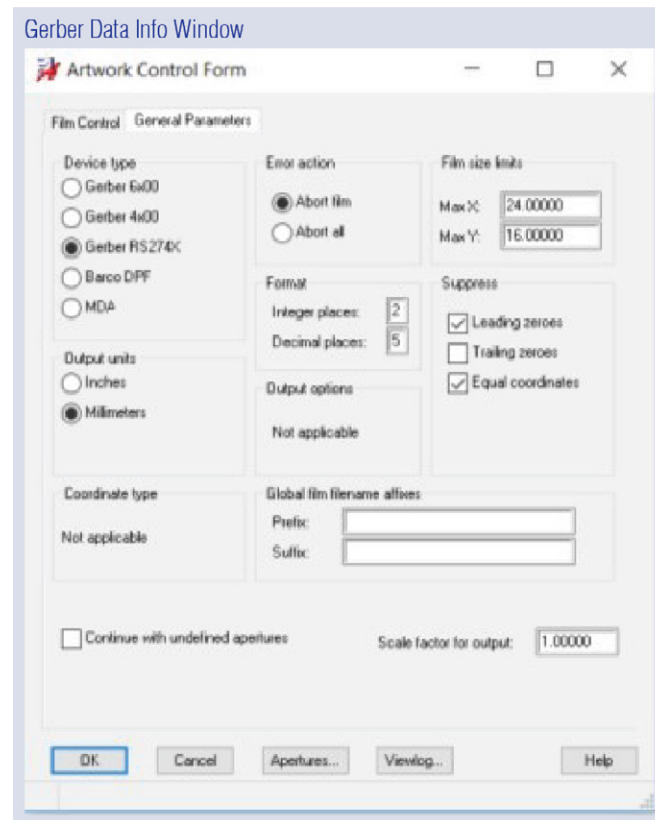
Avoid using non-descript or vague names like “TOP.GBR” for files. Without specificity a data file name will surely be confused as to its purpose. As shown in the examples above, incorporating a part number and revision into the file name links the file to a document control system. Adding a clear functional description to the filename will surely help anyone using the data to realize what its purpose is without having to view it.

Part Number, revision, and function. Examples:

- 424242_B_LAYER_1.PHO
- 424242_B_DRILL.DRL
- 424242_B_FABDWG.DXF

Gerber Data Files for All Required PCB Artwork Layers

This is the starting point for graphic CAM tooling. Referred to as “artwork” the supplier modifies this data to conform to their manufacturing capabilities to meet finished feature requirements specified in the fabrication drawing. After the layout is complete, the software can output these files, each of which will become the basis for the etched copper pattern for each PCB layer.



When outputting Gerber file data, use the very common RS-274X output. This selection utilizes special technology referred to as “embedded apertures” to create the artwork shapes.

Industry Standard Design Continuity Verification Output

IPC-2581 or ODB++ design output and an IPC-D-356 format netlist will help the PCB supplier check to make certain the artwork matches the design intent electrically before and after fabrication. The more intelligent and comprehensive the data, the better.

Industry Standard Drill File

A common output format is Excellon. Drill files define the nominal X, Y position of the holes, but keep in mind, the numeric values output from CAD software define the finished hole size, not the drill size. Drills must be larger than plated holes specified to compensate for plating thickness; the supplier will select the appropriate drill size.

Neutral Database File

Providing the source file for the complete design database allows a PCB supplier to access the source data needed to determine design intent. Unlike “dumb” graphic Gerber data, source data provides intelligent data, net names, and connectivity information which can be helpful in determining artwork anomalies and moving the design through the CAM process quickly. Intelligent source database formats are best output in IPC-2581 or ODB++, but some systems accept ASCII output of the original layout database.

PCB Documentation

Finishing the routing, drilling, and design-checking completes only the graphic portion of a design, but there are other aspects of the design which the CAD data cannot address alone. For instance, CAD data defines the shape of an exposed component land, but not the metalized finish. CAD data defines the geometry for solder resist clearance and the graphic strokes for the assembly legend, but cannot define their color or composition. This graphic CAD data is not able to address the material requirements of the PCB, like temperature rating and structure. Graphic CAD data defines mostly geometric, nominal values for the features which are shown and this is critical for a designer to understand. There are no perfect manufacturing operations—every bit of CAD data will be subject to manufacturing tolerances.

How will the effect of manufacturing variance and so many other aspects of the design be addressed? Data and machinery run the PCB process while graphic PCBA documentation is required to start the process. Graphic media is a tangible source for quotation and setup reference. The ability to view the finished PCB using a manufacturing print helps to start the fabrication process with the end in sight. Graphic PCB documentation also helps to close out and finalize the PCB process by giving the inspection stakeholders a graphic example of what the finished PCB will look like and provides notes and specification for its final electro-mechanical configuration.

Pro-Tip from Mike Brown

“Keep in mind the fabrication and assembly drawings each serve two purposes. They help the fabricator and assembler—serving as a guide, showing material basics—but they also serve as an inspection document for the quality assurance personnel.”

The Fabrication Drawing

There are up to thirteen basic documentation elements which will need to be included in the fabrication drawing:

The Fabrication Drawing
Pictorial
Drill Symbols
Drill Chart
Holes Drilled and Routed
XOY0 Datum Feature
Dimensions and Tolerance
PCB Stack-up Detail
V-Score Detail
Tab-Route Detail
Intentional Shorts Table
Board Outline and Thickness
Impedance Specification
Fabrication Notes

Within the outline, holes are represented using symbology.

Pictorial

CAD data must be accompanied by textual fabrication specifications which are best documented in an engineering drawing.

The PCB fabrication drawing serves less to indicate how a PCB is to be manufactured and more to specify how the PCB shall be laid up. CAD data can define nominal values for features such as drill geometry and the PCB outline.

Automated machinery does a remarkable job of performing drilling and imaging until it doesn't—sometimes automated machinery fails. A particle of dust may land on the material during imaging or etching, and plating chemistry may weaken finished copper. How will the final inspection stakeholder know what is intended and what to expect without a clear, pictorially-rich document which specifies the design intent?

A complete fabrication drawing includes a pictorial view representing the PCB outline. Within the outline, holes are represented using symbology. Each hole position is marked with a symbol which is coordinated with a drill chart on the drawing.

Drill Symbols

Drill symbols are shapes or textual characters generated by the PCB layout software to graphically show a hole's position on the PCB. Being a symbol, it can simultaneously be represented in a corresponding drill chart to convey more information. It is important when selecting symbols for drill sizing to always use a unique symbol for each type of hole containing the same attributes. For instance, there may be several .023 [0.58] diameter holes required on a PCB. If the holes are alike with regards to plating requirements and hole diameter tolerance they may be assigned the same symbol. However, if there is a different attribute, such as a non-plated condition or a different tolerance requirement, the hole of the same size will require a different symbol which will need to be reflected on the drawing accordingly.

Drill Chart

Comprehensive requirements for all drilled holes shall be shown in a drill chart as referenced below. PCB layout software will automatically tabulate all the pad stacks containing holes in the design and reflect them in a drill chart to display the symbols, quantify the counts, display the nominal hole diameters, show the plating requirements, and indicate the diametrical tolerance values which may be obtained by high speed drilling.

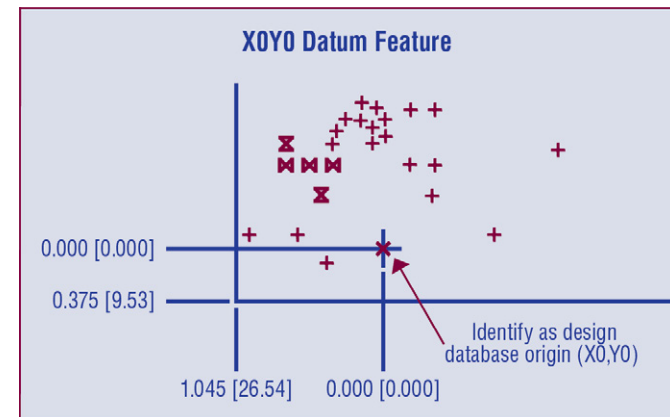
Drill Chart					
Symbol	Count	Hole Size	Plated	Hole Tolerance (+)	Hole Tolerance (-)
✕	262	10.00mil (0.254mm)	PTH	3.00mil (0.076mm)	10.00mil (0.254mm)
●	20	32.00mil (0.813mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
■	6	29.00mil (0.737mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
▼	4	107.09mil (2.720mm)	NPTH	3.15mil (0.080mm)	3.15mil (0.080mm)
+	2	102.36mil (2.600mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
	294 Total				

A special note here to PCB designers about specifying holes. It is useful to understand how a specified hole will be formed to determine if it even belongs in the drill chart. Most fabricators will limit drilled hole sizing to less than .250 [6.35] diameter. Therefore, hole information destined for the drill chart shall be extracted from a corresponding pad-stack which automatically places the information there. To avoid manufacturing confusion, only holes to be drilled shall be listed in a drill chart. However, there are many reasons to use holes greater than .250 [6.35] diameter. How are those holes specified and manufactured? The answer here is to consider larger holes as internal board edges. How are board edges machined? The routing option is utilized here to route the edge profiles of both board edges and holes. When designing

a hole larger than .250 [6.35] avoid using a pad-stack. Better to use your software's "board cutout" function to design this shape. Be aware while tolerances for drilled holes can be held tightly to $\pm .003$ diameter due to their machining operation's accuracy, holes formed by a routing operation are usually expected to be less tightly maintained; only subject to the expected tolerancing of the board outline.

XOYO Datum Feature

The XOYO Datum is a hole on a PCB which is preferably located in the lower-left corner of the design.



During the fabrication process, machinery and process will stray from specified nominal target dimensions by various amounts.

Dimensions and Tolerances

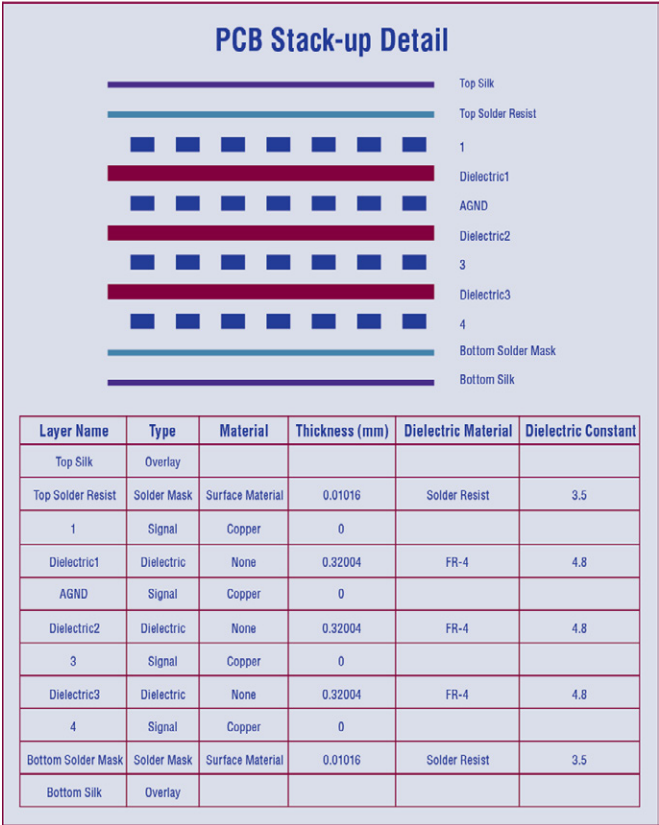
Designation of the origin point (X0Y0) for the design database s relative to practical interface points on the PCB. Dimensions and tolerances shall originate from X0Y0 on the PCB.

Fabrication drawing dimensions do little to communicate to the supplier how to fabricate the PCB; the PCB design tool output (CAM) data does this. Fabrication drawing dimensions are used by manufacturing and inspection personnel to gauge the accuracy of the process and machinery. During the fabrication process, machinery and process will stray from specified nominal target dimensions by various amounts. How much is acceptable? This is an important design question which must be addressed by the designer. Accuracy, expressed by the definition of tolerance values, must be documented on the fabrication drawing for the supplier to measure their success and adjust the process as required. CAM data does not include the establishment of tolerance zones and therefore has no bearing on whether a snap-fit feature will work at next assembly. Successful fit can only be ensured by proper consideration and assignment of dimensions and tolerances to the PCB features on the fabrication drawing. These dimensions must be derived from the mechanical engineer.

PCB Stack-up Detail

A stack-up detail provides imperative, up-front, cost-related information to your purchasing department and the supplier's quoting department before the fabrication process ever begins, whether the design is a simple, single-sided PCB or a complex multi-layer design. This detail serves the purpose of documenting a generic view of the vertical design intent—the layer count, the thickness of the copper layers, the dielectric

materials in between, and the presumed thickness and dielectric properties of the solder mask material covering the outer-layer surface copper. For controlled impedance, adopting a stack-up philosophy which allows the board supplier to vary the dielectric constant of materials, trace widths, and spacing to achieve the specified impedance is recommended. This will allow usage of materials with wider availability, especially off-shore, and is critical to improving the supplier's ability to deliver the highest performance at the best cost.



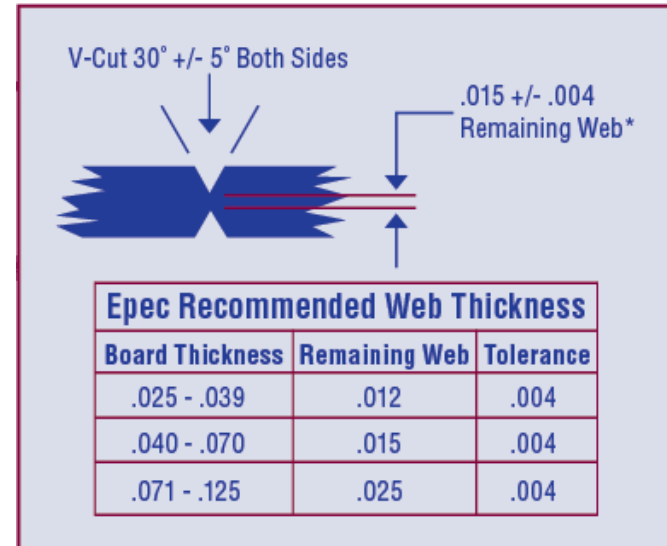
Panel Processing

When the PCB design is set up for panel processing, the PCB image is multiplied several times in order to process many PCBs on the same manufacturing panel to maximize yield of the panel. Yield here is used as the term to express how many PCB images a supplier can fit on a panel.

If the PCB you are designing will be fabricated and assembled outside of your facility, you will not have to utilize a V-Score or a tab-route detail. These will be added by the suppliers.

V-Score Detail

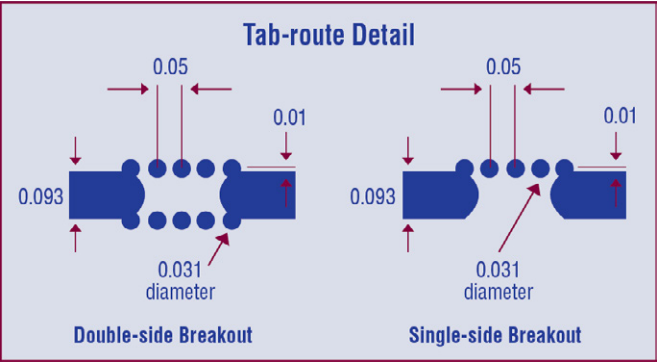
Typically, it is uncommon to provide a V-score detail on a fabrication drawing. A fabrication drawing should describe the finished part and therefore should not show extra processing material unless required. If a V-Score detail is required, it is because the project stakeholders are intending that the PCB will be processed in-house, in which case the in-house assembly stakeholders will need manufacturing assembly arrays with V-Score cuts between the straight edges of the PCB to provide rigidity during the assembly operations. The V-Score detail needs to be shown alongside the PCB array view so it can easily be referenced by simply adding (V-Score) to any straight edged PCB feature with the requirement. Otherwise, they can be left for the suppliers to decide. It's best to always check-in with both the assembly house and the fabricator for optimal v-score parameters.



Tab-route Detail

Like the V-Score detail, the tab-route detail is only provided if there is in-house assembly processing. Tab-routing is used to support the PCB in the assembly array with short break-away tabs when straight edges are not available on the PCB or a smooth (routed) machine finish is required. The tabs are formed by a router bit which cuts a slot between the board edge and any excess material on the panel. At pre-determined intervals the route slot is stopped. The tool is lifted, moved ahead slightly on the route path and then re-plunged to form another slotted route path. The resulting material between the slot ends is called the tab which serves with as many other tabs as required to support the PCB within the PCB array.

The best source for tab-route detail info is the assembly supplier, because they control the end purpose process of excising (de-paneling) the individually assembled PCBAs.



Intentional Shorts Table

Sometimes it is necessary to connect multiple signals together in a design at a specific point (for example: analog GND and digital GND). This methodology creates a common problem for most CAD software tools because this condition is normally referred to as a “short” and they are very good at checking for these. When a net with a specific name needs to connect with another net having a different name, a designer will often use a ‘bond’ part to connect the nets. This bond is a copper shape that makes the connection and can trick the design rules checker. However, when the connected copper shapes are compared with the IPC-D-356 netlist, a red flag is raised at the PCB supplier’s CAM department. The very common practice of net joining will almost always cause a stop order to a job, unless it is described on the drawing in detail. The supplier does not know if the ‘short’ between multiple nets is intentional or not. An Intentional Shorts Table can be used to effectively communicate the important information of bond reference designator, net-names, XY location, and layers to the supplier’s CAM department up front; reducing the need for stop orders.

Intentional Shorts at Following Locations:				
Ref Des	X Loc	Y Loc	Layer	Signals
BND1	4.400	0.200	1	3V3OUT/+3.3V
BND2	9.175	0.425	1	+14.3V, 14V3OUT
BND3	6.490	0.025	1	2V5OUT/+2.5V
BND4	9.250	1.500	1	VLEDOUT/VLED
BND5	7.125	0.050	1	1V4OUT/+1.4V

PCB thickness, however, is not confined to fractional equivalents.

Board Outline and Thickness

Overall PCB length and width may be shown as reference on the fabrication drawing if the features need not be inspected. A note pertaining to the minimum radius for internal corners and overall profile tolerance may be specified in the fabrication notes.

Traditionally, PCB thickness was expressed in fractional equivalents, for example: $1/32" = .032$, $1/16" = .062$, $3/32" = .094$, $1/8" = .125$, etc. PCB thickness specification continues to follow this standard today because many mating part interfaces – pin lengths, connector slots, etc. —are designed to accept these standard thicknesses. PCB thickness, however, is not confined to fractional equivalents. Utilizing various lamination techniques, PCB thickness can be laminated up to any reasonable thickness. Core and pre-preg materials come in a wide array of thickness, but as thin as .0025[0.06]. It is possible to spec for example, .016[0.41] or .048[1.22] as the PCB thickness and have it produced by almost any supplier. Many suppliers can produce a PCB with a tolerance range of $\pm 10\%$ for .039[0.99] thickness and greater in addition to a $\pm 15\%$ range for a PCB thickness less than .039 [0.99].

Impedance Specification

Impedance-controlled designs require control of four physical variables in the stack-up:

- Trace thickness
- Trace width
- Trace distance from reference plane(s)
- Dielectric value of the material

A designer may use a basic field solver or off-the-shelf impedance calculator to determine trace widths and spacing to be used in the design for impedance requirements. At the start of the layout, the designer should do a feasibility check to select the optimal trace widths for impedance-controlled lines; be sure to validate the values in the stack-up with the PCB supplier. Designers should use care when adding information to the stack-up detail regarding three of the four variables mentioned above. Finished copper thickness is an important consideration regarding the various conductors' current-carrying capacity. However, the values of trace width, distance from reference plane, dielectric constant of the material (E_r), and material sources should be allowed to be adjusted by the supplier for best DFM.

Caution: Using the stack-up detail to 'document' the recipe for a successfully performing PCB prototype may set a design up for procurement challenges. This is because some custom hybrid materials used by local prototype shops to "dial in" the impedance may not be readily available off-shore.

Impedance Calculator

Conductor Impedance

Conductor Width (W) mils Conductor Height (H) mils Frequency (MHz)

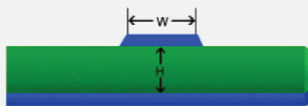
Er Effective = 3.0856

Zo

Lo

Co

Tpd



**Note: This calculator can be found on satumpcb.com*

Fabrication Notes

Some common PCB process notes are included here as minimal expectations for most manufacturing suppliers. It is up to the designer to adjust modifiers in the notes accordingly.

1. Designate the primary side of the board.

The primary side of the board is the side the designer has designated as such. The document pictorial shall show the board design oriented, so the primary side is viewed from the top and all subsequent layer views are oriented looking through the design (non-mirrored).

Example: Primary side of board is shown.

2. State manufacturing, qualification, and performance.

Manufacturing, qualification, and performance for class 2 (dedicated service electronics) is described in IPC-6012, while acceptability (inspection) criteria is covered in IPC-A-600. Both specifications fit together in this note to define quality.

Example: Printed circuit board fabrication per IPC-6012, Class 2 Except as specified herein. Acceptability of printed circuit board per IPC-A-600, Class 2.

3. Define materials.

Unless there is a good reason, it is best to allow the supplier to use their preferred glass-epoxy resin system using any glass weave, conforming to IPC-4101. Variables defined in IPC-4101 are glass transition temperature (Tg) and delamination temperature (TD), which have values acceptable for RoHs manufacturing temperatures. Copper foil is rolled and annealed as provided to the PCB manufacturer. During the plating process, electrodeposited copper is added to the base copper. The base copper foil (finished = etched or plated) can be noted in the stack-up detail.

Example: Materials: Plastic sheet laminated, glass base, epoxy resin type FR4 series or equivalent per IPC-4101 with a Tg $\geq$ 170 DEG C and a TD $\geq$ 330 DEG C. Base thickness on all layers per stack-up detail.

4. Define overall board thickness.

PCB thickness is specified and controlled in the notes. An acceptable tolerance for boards of this thickness is considered $\pm 10\%$. PCBs are constructed in various ways and thickness does not have to be held to the traditional .031, .062, .093 decimal fractional equivalents. Core construction or foil construction using layers of pre-preg material combined with sheets of copper foil can yield almost any thickness requirement.

Example: Overall board thickness shall be .063 $\pm 10\%$ [1.60 $\pm 10\%$].

5. Define UL rating.

Underwriters Laboratories (USA) flammability rating requires any burning on a vertically-mounted test PCB stops within ten seconds. This testing is required on PCB's utilized in most industries.

Example: Finished board shall have a UL rating of UL 94V-0.

6. Define impedance.

Identify the layer, line width, impedance value, and tolerance of a trace to be controlled. Identify significant lines by assigning them a unique width so they will not to be confused with uncontrolled lines. A 6.1 mil wide line can easily be identified and will stand out from numerous 6 mil wide lines when viewed in CAM processing software.

Example: Impedance shall be as follows (example):

Layers 1 & 6 – 60 ohm +/- 10% single-ended on .007 [0.15] wide lines.

Layers 3 & 4 – 60 ohm +/- 10% single-ended on .005 [0.13] wide lines.

Layers 3 & 4 – 100 ohm +/- 10% differential on .0045 [0.114] wide / .0095 [0.241] spaced lines.

7. Define an etching and plating tolerance.

A tolerance requirement helps to control the finished width of a copper feature, while giving the supplier a range to work with when compensating lines for impedance control. It is important to keep the least material condition of this tolerance in mind when calculating the current-carrying capacity for conductors. Allowing a supplier to add thieving patterns to unused areas of the layer plane can help them to accomplish accuracy and consistency throughout the etching and plating process.

Example: Etching / Plating tolerance: +/- 20% from supplied Gerber images .010[0.25] or less. +/- .002[0.05] from supplied Gerber images .010[0.25] or greater. Supplier may utilize thieving to compensate for low copper density on this design. Thieving pattern clearance shall be as follows: Thieving to adjacent copper, all layers: .100[2.54] min. Thieving to fiducials and non-plated holes: .050[0.13] min.

8. Indicate copper plate holes and conductors.

This specification provides an adequate amount of copper plating for average-sized holes in boards with an aspect ratio of 10:1 and below. This is deliverable by most suppliers. It is very important to consider this plating amount when determining finish copper thickness for conductors. Make calculations for impedance and current-carrying capacity based upon finished copper values.

Example: Copper plate indicated holes and conductors .0010[0.025] Average—.0008[0.020] Minimum.

9. Include fabricator information.

Vendor Option: The above may be added using epoxy ink on the legend layer if board size or copper pattern does not allow for etching. Fabricator information pertaining to note nine is traditionally added onto the secondary side of the PCB, but may be added anywhere if a location is not designated on the fabrication pictorial.

Example: Etch manufacturer's name, date code, initial or trademark (logo), followed by a code number or equivalent designation and UL rating of 94V-0. Avoid all copper images and by .050[1.27] Minimum.

10. Define location tolerance for smaller holes.

Locational tolerance for smaller holes (non-mounting or non-tooling) is specified in this note. Expressed in the shape of a circle, the tolerance diameter of .008[0.20] allows the hole radius to wander .004[0.10] in any direction from its nominal center-point, relative to the drill pattern's 0, 0 origin. Holes larger than .250[6.35] are typically routed (not drilled) and need tolerancing like those applied to a routed board outline edge. A routed hole creates a board outline.

Example: Drilled holes without lateral dimensions shall be located within .008[0.20] Diametric True Position from nominal location specified in drill data files.

11. Define finished hole sizes.

It is important to reference this chart as a drill chart containing only holes (typically less than or equal to .250) which are drilled. It is a common mistake to list larger holes requiring routing in this chart, which confuses the machining operations. For designs requiring blind and buried vias, it is important to incorporate a separate chart identifying holes making layer-to-layer connections internally.

Example: Finished hole sizes are shown in the drill chart.

12. Designate the controlling performance specs for the solder mask.

IPC-SM-840 is the controlling performance spec for solder mask. Commonly applied over bare copper and referred to as Solder Mask Over Bare Copper (SMOBC). The most common solder mask color is green; however, it can be ordered in many colors and finishes. Class specification is described as telecommunication (T) or high reliability (H).

Example: Apply green LPI solder mask, matte finish, conforming to IPC-SM-840, Class T, over bare copper onto outer surfaces using appropriate artwork.

CAD data will not automatically color the solder mask to be blue or the legend ink to be yellow.

13. Define silkscreen manufacturing methods, if applicable.

Commonly referred to as “silkscreen” the legend is applied to identify components and mark other important information onto the PCB. Silkscreen manufacturing methods are rarely, if at all, used anymore. The process has been replaced by faster and more accurate printing methods such as ink-jet technology.

Example: Apply legend onto primary / secondary surfaces as required per supplied Gerber artwork. Color White.

14. Define finishing processes

The two most common methods of cutting a board edge are routing and V-Scoring. Routing is performed by a cutter on a spindle machine, resulting in an accurate, sealed edge of most any shape. V-Scoring is performed by a saw blade and is limited to straight cuts. The V-Score operation leaves a rough edge that can wick moisture, but is preferred for volume production. The designer must be aware of the differences between these two finishing processes when assigning tolerance values to the board edge features. A profile tolerance of .005[0.13] is considered acceptable by most suppliers using either process.

Example: PCB edge profile shall conform to supplied Gerber data within .005[0.13].

15. Define internal corners.

The process of V-Scoring cannot cut curved PCB outline paths; internal corners must be routed. Typical route sizes are .039 - .079[1.00 – 2.00] diameter. Tool size must be considered when specifying an internal corner. A large radius is easily cut, but a small radius greater than or equal to .039[1.00] will impact the suppliers options due to tool availability.

Example: All internal corners .039[1.00] R Maximum.

Conclusion

CAD/CAM data has replaced the need for human contact with the features comprising the finished PCB during manufacturing cycles. Manufacturing stakeholders rely on data automation and machinery to create some fine lines and complicated mechanical PCB features.

A problematic assumption made today is that manufacturing processes and machinery create hardware which perfectly matches the nominal design layout. This is not true. Due to manufacturing tolerances, every manufacturing process is subject variants which yield features which are under-cut or over-cut—under-etched or over-etched. If the accumulation of tolerance ranges in an assembly is disregarded by the designer the assembly may fail to assemble due to interference or fail to align accurately due to too much clearance.

Design data has other short-comings. CAD data will not automatically color the solder mask to be blue or the legend ink to be yellow. Embedded CAD data will not automatically select RoHS materials or automatically pull high temperature grade material into a stack-up during the lamination phase.

Therefore, the fabrication cycle still relies heavily on textual and graphically detailed information provided on a comprehensive fabrication drawing.

A sufficiently embellished fabrication drawing including the graphic and textual information provided in this chapter will fill in the blanks that embedded design data leaves out. And while CAD/CAM data tells the supplier's machinery what to do, graphic and textual information provided on the fab drawing will guide the inspection department in checking how well it did.

Tips for Fabrication and Data Documentation

- ☐ CAD data must be accompanied by textual fabrication specifications which are best documented in an engineering drawing.
- ☐ Add common PCB process notes as minimal expectations for most manufacturing suppliers. It is up to the designer to adjust modifiers in the notes accordingly.
- ☐ Add process documentation standard details reflecting stack-up, drill chart, v-score or tab-route if panelizing.
- ☐ If intentional shorts exist in the design, make sure to show the X,Y layout location and net names using a table to answer the supplier's query before they even have to ask.
- ☐ Remember every process yields a physical feature which will vary in size from the nominal intent. Make sure to specify a meaningful tolerance for every feature that must interface with another at next assembly.
- ☐ Choose an existing non-plated mounting hole in the layout or add one in order to designate an X0,Y0 origin for the PCB layout.
- ☐ Designate holes $\leq .200$ to be drilled. Designate holes $> .200$ to be routed. Drilled holes may be held to tighter tolerances. Routed holes are in fact board edges and should match board edge tolerancing.
- ☐ Specify board outline tolerancing as a profile tolerance in the general notes. Work with mechanical stakeholders to allow a PCB thickness tolerance of $\pm 10\%$ for boards .039[0.99] thickness and greater and $\pm 15\%$ range for a PCB thickness less than .039 [0.99].
- ☐ Add impedance control specification as required by calculating the trace width, distance from reference plane(s), and dielectric value of the material using a simple impedance calculator. Check in with the supplier to verify your values. Do not let the supplier adjust traces thickness (z-height) as part of the equation because it can have an adverse effect on current carrying capacity for that layer.
- ☐ Make sure all required output data for fabrication is included in the manufacturing data package.
- ☐ Include a complete fabrication drawing in the manufacturing data package.
- ☐ If your company intellectual property rules allow, output formats of IPC-2581, ODB++, or ASCII, and include the source design database in the manufacturing database.
- ☐ Include Gerber data for all required artwork layers.
- ☐ Include industry standard, Excellon drill files which reflect finished hole sizes.
- ☐ Always use a tangible naming convention for your manufacturing files in the form of part number, revision, and file function.
- ☐ Always check in with the supplier stakeholder regarding special material processing and availability not only in prototype but for production too.
- ☐ Keep up to date regarding processes and capabilities by keeping in frequent touch with your PCB supplier.

Chapter 10

Assembly Data & Documentation, Process Overview

From start to finish, Ian saw proper design consideration is critical for supplying viable data and documentation to drive the hundreds of steps involved in fabricating a PCB at the board shop. With the help of the assembly and test stakeholders, Ian was amazed to discover that the viable data driving the PCB assembly processes after the PCB is fabricated is just as important.

After the PCB layout is complete and the data and documentation for the PCB has been generated, the fabrication package has most likely been released for fabrication. PCB fabrication cycle, or turnaround time, can vary depending on whether the design is being considered for quick-turn or standard fabrication. Quick-turn times for PCB's can be accomplished at specialized PCB fabrication shops and are measured in days, sometimes hours. Standard times are typically measured in weeks. Timing of the PCB fabrication cycle is mentioned here because it is a good indicator of how much time a designer needs to finish his or her final project design responsibility and generate assembly data and documentation.

Data drives the process. It is very important a complete package of data is supplied to the assembly stakeholder. As in any other process, without complete and accurate data, the process will stall or become confused, resulting in time-consuming queries between the supplier and the customer. The following describes the main items of a complete assembly data package.

Assembly Data Package

Bill of Materials File

Neutral Database File

X,Y Placement File

Solder Paste Stencil Artwork File

Test Point Location File

The Bill of Materials File (BOM)

After investing so much thought, effort, and time into the layout it is sometimes hard for a designer to consider that once the PCB is fabricated, it will simply be treated as another component commodity—one which must be ordered along with many other components. This will then feed into the PCBA using the BOM.

The assembly process starts with the evaluation of all materials published in a BOM report which is exported as data output from the schematic end of the design and layout process. A BOM which lists all PCBA components, their manufacturing part numbers, descriptions, and corresponding reference designators is a powerful tool for use by a supplier management purchasing agent. The sooner the component information can be captured and sent to them, the better. Challenges will arise and can include item costliness, long lead time, discontinuation, and obsolescence. The ability to flag potential procurement problems requires visibility.

The exported BOM must list all the electronic and mechanical parts used in the assembly, including the bare PCB, all components, and even mechanical hardware, adhesives, coatings, and wire. The EMS planning department will start with this important list to check for two very important attributes: availability and cost. If the EE has checked for these two important component virtues during the front-end design of the PCB layout, everything should go quite well and even better if the EMS supplier negotiates volume purchasing discounts for the components.

The Neutral Database File

Provision of a neutral CAD database is just as important to the assembly provider as to the PCB supplier. A neutral database such as ODB++ or IPC-2581 is leveraged differently by the assembly supplier. AMEs base their BOM checks on comparisons with intelligent manufacturing data provided in neutral formats such as IPC-2581 or the widely-used ODB++ format. Once all the design for assembly (DFA) checks are complete and the PCB assembly process begins, all the parts are kitted and moved forward to be assembled onto the bare PCB.

Source data provides intelligent data, net names, etc. These can be helpful in sorting out component placement, orientation anomalies, and moving the design through the placement CAM setup process quickly. Intelligent source database formats are best output in IPC-2581 or ODB++ because they provide the most usable information to the board fabricator and assembly processor.

Pro-Tip from Patrick Davis

“Everything is derived from from ODB++ data: Our MPI (Manufacturing Process Instructions), DFM (Design for Manufacturability analysis), Programming, AXI (Automated X-ray Inspection), AOI (Automated Optical Inspection), Final Inspection. All the work done on the SMT machines is first analyzed for DFM by taking in the ODB++ data and the BOM data. We compare the two together and make sure they match. This foundational part of the DFM process will make sure we can build the PCBA. In effect, the data allows us to model a virtual preliminary build. It allows us to experiment with different processes to determine which one of many will yield the best results.”

The X,Y Placement File

The X,Y placement file, commonly referred to as a “pick and place” file, is the output data which will be used by the assembly stakeholder to program the placement machinery. The file output can be very simple ASCII text data, but must include enough information for the operation to run smoothly.

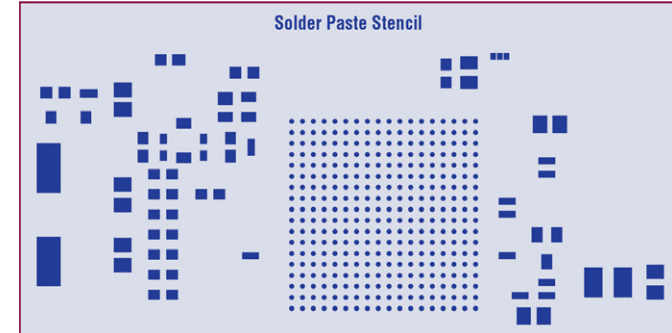
Placement output can vary regarding output format and order of data columns. As with all things PCB and PCBA, check in with the assembly stakeholder regarding their preference. For each part to be placed, the X,Y placement file needs to specify a reference designator, side of placement, X,Y location and angle of orientation.

Pro-Tip from Mike Brown

“I am an advocate of supplying ODB++ or IPC-2581 files. It is important to provide the manufacturer with some type of comparison data to check their work against the design. However, this practice is a two-edged sword—while helping the fabricator or assembler by providing all of the component information and pin information along with all of the connectivity, you must trust that the design will not fall into the wrong hands. There are software tools out there which can easily use this comprehensive data to reverse-engineer the design and basically convert the data back into a CAD database putting your intellectual property at risk. Regardless, if the design database is archived in a neutral format there is a benefit that your company can update the design in the future, even if they change layout tools.”

Solder Paste Stencil Artwork file

Before any SMT parts can be placed upon the board, the PCB must run through a process which will deposit a thin layer of solder paste onto the component footprint lands which have been etched and plated onto the outer layer(s) of the PCB. This process will be described in more detail later in the chapter, but to apply the solder paste accurately, a thin metal stencil must be manufactured by a special manufacturer which specializes in etching and electroforming thin sheets of stainless steel. A solder paste stencil artwork file is usually output in Gerber format from the source design layout and includes all the required openings to allow solder to be screened onto the SMT lands.



Important tip for the designer: Provide 1:1 land geometry for each intended SMT land. Do not attempt to compensate. Again, the PCB designer does not know the EMS provider's variable manufacturing process criteria, so stencil opening definition, including compensations and special “home plating” techniques are best left to the stakeholder of the process.

Test Point Location File

If testability will be implemented on the PCBA, a file will need to be included to define all the test point locations for the test fixture supplier to build the equipment. Like the placement file, the test point output file can be very simple ASCII text data. The file is output from the source design layout and derives its data from test point lands which have been specifically identified for test. The file needs to include net names, side of access X,Y locations, and test point names if applicable.

It's hard to believe, but all the automated machinery involved in making a small prototype run of PCBAs, all the way to up to making production runs of millions of PCBAs, can be programmed to run by using only the five data files mentioned above. However, as fast and accurate as modern assembly process machinery is today, there remains manufacturing variables like temperature variations, material inconsistencies, component damage, and tool wear which can cause perfect machinery to make mistakes. As has been echoed throughout the context of the chapters within this book, nothing is perfect—everything has a tolerance. There must be a vehicle to graphically define the limits of acceptability for the PCBA. Like a bare PCB needs a fabrication drawing to define these things, a printed circuit board needs an assembly drawing and documentation to complete the assembly and inspection process.

Test Point Coordinates

```
bottom_probe.drl - Notepad
File Edit Format View Help
;LEADER: 12
;HEADER: none
;CODE : ASCII
;FILE : C:/Users/shannonh/Desktop/Assignments/Battle_Cards/Battlecards6/artwork/bottom_probe.drl
G00
X01450Y03640
X01470Y04160
X01485Y03759
X-00059Y03801
X-01717Y00445
X01505Y03110
X04757Y-00412
X01540Y-04365
X02618Y-04755
X02618Y-04855
X-01667Y-00127
X-01658Y01858
X00490Y03640
X04814Y-02106
X04814Y-02006
X03744Y-01941
X03744Y-01539
X03744Y-01205
X03744Y-00803
X03744Y-00602
X03744Y-00535
X03744Y-00468
X03744Y-00402
X03744Y00201
X03744Y01004
X03744Y01339
X03744Y02075
X03744Y02476
X03744Y02610
X01605Y03110
X04838Y04088
X00561Y03097
X-00510Y-02020
X00577Y03753
X01655Y04055
X03807Y-01640
X03807Y-01573
X03807Y-01037
```

PCB Documentation is often one of the most disliked tasks a designer has.

PCBA Documentation

Though data and machinery run the PCBA manufacturing assembly process, complete, graphic PCBA documentation begins the process. Tangible documentation reflecting what the data will produce is critical for quotation and setup reference.

A complete PCBA document gives manufacturing stakeholders the ability to view the finished PCBA and start the assembly process with the end in sight. Additionally, the same helps to finalize the PCBA manufacturing process by giving the inspection stakeholders views and notation with which to evaluate the finished product.

As we have discussed, PCB Documentation is critical to manufacturing success yet, it is often one of the most disliked tasks a designer has. A few layout suites and third-party PCB documentation programs are incorporating advanced documentation toolsets which are easing the documentation process workflow.

By having the capability to access all the source layout data, the tools can create extremely detailed, dynamic views of the PCB assembly in which scaling takes seconds, special magnified views of very small parts can be highlighted into a detail bubble, and even generate specialized reference designators for the cause. The power of these next generation documentation tools can now even access the inner layers of the PCB to show traces which might need to be cut or jumped and perhaps even a rework routine. Documentation tools which can reduce the drafting time cycle while ensuring the quality you need to drive successful manufacturing are worth checking into.

There are basically three elements of PCBA documentation:

PCBA Documentation

The Schematic

Bill of Materials

Assembly Drawing

The Schematic

Documentation for the schematic is most likely the simplest act of PCB documentation. Since the schematic served as the source design file driving the layout of the PCB, the schematic becomes a “document” by simply placing a proper format around it. How this is provided, whether through a source file, paper copy, or PDF is usually dependent on company culture. Formalization usually involves obtaining approval signatures and submission to a company release and distribution process. There are typically no extra details added to the schematic at the time of formal documentation.

The Bill of Materials (BOM)

The BOM documentation is an official, formatted document which may be embedded inside a complex, corporate data management system. Documentation for the BOM is always output from the source: the schematic document. The part line items are pulled into a paper or electronic environment which allows for signature approval and formal release for distribution to purchasing, manufacturing assembly, and inspection stakeholders.

Assembly Drawing

Like the PCB fabrication drawing explained in the previous chapter, the PCB assembly drawing serves less to indicate how a PCBA is to be manufactured and more to specify how the assembly shall perform.

The job of the PCB assembly drawing is to show all the parts which will be assembled onto its two outer surfaces. It is used as a guide for placement programmers and inspection personnel to measure how well the parts were placed on the board, how well the solder joints were formed and how clean they must be at the end of the process.

Again, automated machinery does a remarkable job of executing assembly tasks, until it doesn't—sometimes automated machinery fails. A part may be installed backward or tombstone. How will our final inspection stakeholder know what is intended and what is expected without a clear, pictorially-rich document which specifies the design intent?

To serve as a viable manufacturing reference, the complete assembly drawing needs to include at least three key items to satisfy the needs of the assembly manufacturing stakeholders:

- Assembly Pictorial
- Assembly Details
- Assembly Notes

This is often the circumstance on PCB assemblies that are dense with small parts.

Assembly Pictorial

The pictorial starts with a view of the PCB outline showing all the component outlines and their respective reference designators. The assembly view can be imported into a 3rd party documentation tool or created right inside the PCB layout. However, the designer needs to understand the assembly document must be able to be printed and read by any stakeholder at any time. The most important thing to consider here is legibility. If the assembly is large and uses large components, a one-to-one (1:1) scaled image may be all that is required if the reader can see all of the parts, their orientation and their reference designations. If parts are to be installed on two sides, a secondary side view must be depicted. If the PCB assembly is small and dense and contains many SMT parts, a larger scale of 2:1, 4:1 or larger may be used to show the assembly.

However, there are often extra processes such as mechanical hardware torquing requirements and post-op applications of adhesives and selective epoxy coatings which may need to be applied that may require more detailed depictions.

Assembly Details

Assembly details are required when there is not enough information provided on the main pictorial. This is often the circumstance on dense PCB assemblies with small parts. Sometimes there is just not enough space left over for reference designators to be printed on the PCB. In this case, the reference to the parts must be documented on a scaled assembly detail. Example:

Assembly Notes

Some common PCBA process notes are included here as minimal expectations for most manufacturing suppliers. It is up to the designer to adjust modifiers in the notes accordingly.

1. Designate the primary side of the board.

The primary side of the board is the side the designer has designated as such in the PCB layout. As designated in the PCB fabrication drawing, the primary side designation should follow through to the PCB assembly drawing for consistency. The document pictorial should show the board design oriented so the primary side is viewed from the top. If the PCB assembly includes parts on two sides (both primary and secondary) an additional view showing the secondary side shall be projected onto the layout view.

Example: Primary side of the board is shown.

2. Define reference designators.

Reference designators are commonly printed onto the PCB; however, stakeholders can forget the printed alpha-numeric markings are printed onto the PCB for reference. Sometimes, when there is no space for them, they are not there at all. It is the PCB assembly document which allows space for all of the assembly markings to be displayed.

Utilizing the scalability of a good assembly drawing view, component designators can be shown in their full glory. They must be legible and positioned within the part outline to provide guidance to assembly, inspection, and field service personnel who will be using the drawings during their duties.

Once the assembly image is documented, the markings become part of the assembly and inspection process.

Example: Components are identified by matching reference designators in the parent bill of material and with those on the face of drawing. PCB Reference designators are for reference only and may not appear on the PCB or part.

3. Specify Mounting Instructions

IPC-CM-770 Guidelines for printed board component mounting is a specification whose purpose is “to illustrate and guide the user seeking answers to questions related to accepted, effective methods of mounting components to printed wiring boards.” Including this specification on the assembly drawing can add clarity between the customer and supplier regarding industry-accepted methods for assembly without micro-managing which process is used by the supplier. Additionally, IPC-A-610 is included as a manufacturing acceptance specification which—regardless of the assembly method used—will define the acceptance criteria for all assembly operations.

Example: Printed board component mounting shall conform to IPC-CM-770. Acceptability of this electronic assembly shall conform to IPC-A-610, class 2.

4. Specify Soldering Instructions

J-STD-001 serves as the authority for electronics assembly soldering worldwide. It describes materials, methodologies, and verification requirements for all aspects of creating high quality solder joints. The J-STD-003 specification is the industry accepted standard for testing all aspects of the practical contents of J-STD-001 and includes helpful defect definitions and illustrations. The two specifications work together within an assembly note to ensure quality interconnectivity.

Example: Solder per J-STD-001 and J-STD-003.

5. Note any specialized assembly methods.

Unless the PCB you are documenting is being used for military, space, or other exempt criteria, the specified manufacturing processes and material used on your PCBA will no doubt require specialized assembly methods which are free of lead. The environmental specifications and requirements for lead-free assemblies are usually documented far upstream in the documentation channels such as the parent bill of materials. The special marking method which is required for such assemblies is defined in IPC-1066.

Example: Assembly shall conform to environmental requirements in parent bill of material. Mark assembly with category (categories) of solder material used in accordance with IPC-1066.

Fabrication Vs. Assembly Documentation

Compared to having to specify the thousands of holes, traces layers, and processes involved with bare PCB documentation, the documentation for a PCB assembly appears simple. The ones who will be finishing and inspecting the PCBA are going to appreciate the time you spent on the front-end. If you have successfully completed and ensured the accuracy of your schematic and bill of materials, the efforts will have served to “pay it forward” as they are fed into the creation of a clearly illustrated, detail-rich, and simply-notated assembly documentation to serve the needs of the assembly, test, and field service stakeholders.

Since hitting the “send” button after completion of the PCB design layout (as Ian did in our story) weeks, days, or only hours may have passed before the send button will once again be hit to send the PCB assembly data and documentation to the EMS supplier for the boards to be assembled. The difference between Ian’s experience and yours (as a designer who has learned from his mistakes) will be striking. Sure, there will be phone calls before and after the data is sent, but they will not involve the chaos and emergency of an assembly line shutdown. Exposure to the information in this guide along with a willingness to reach out to the people in the EMS industry who perform the work, many phone calls will be positive and inquisitive from the designer to the stakeholder as a pro-active means of preventing manufacturing problems rather than fixing them.

Pro-Tip from Mike Brown

“Find a mentor. A degree doesn’t mean you know it all. There is always something to learn because PCB technology is constantly changing. A PCB designer must be willing to accept and deal with change. Stay in touch with the people on the forefront of this technology—the fabricators and assemblers. Establish a good relationship with them and tour their shops. You’ll learn something new every time you speak or visit.”

As surprising as it is to find many PCB designers have never stepped foot into a PCB fabrication shop, it is probably true just as many designers have never walked the floors of an EMS supplier to get in touch with how the PCBs are assembled. For the designer who has not had the eye-popping experience of watching the PCB assembly process, a brief overview of some basic assembly processes are presented here. The topics mentioned here are by no means intended as a substitute for witnessing the processes in action. As we’ve encouraged throughout this text, visit the supplier. Shake hands and learn by watching the actual process.

Assembly Process Overview

Manufacturing Panel

V-Scoring

Tab Routing

Punching

Programming Placement Machinery

Applying Solder Paste

Automated Placement

Moving Through the Reflow Oven

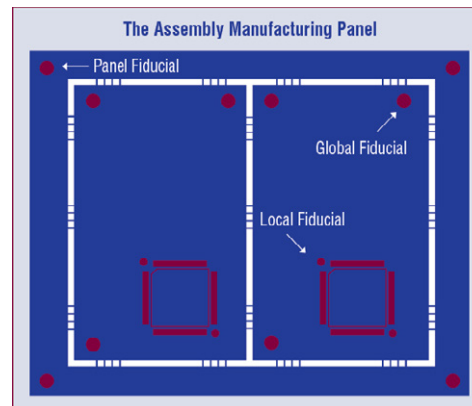
Second Op Assembly Processing

Assembly Test

Final Inspection

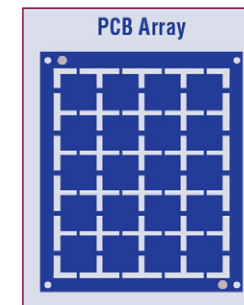
Manufacturing Panel

Every PCB designer needs to be aware that the PCB on their screen at the time of layout will need to be multiplied into an array form (or panel) for volume manufacturing. Modern assembly machinery is designed with sliding rails which can accommodate PCBA widths of a few inches to over 20 inches. This equipment can be very expensive. On a high-volume assembly line, the manufacturing engineers will try to optimize the run time of an entire manufacturing lot of board assemblies, so the machinery can be freed up to run the next job. It would not make good manufacturing sense to run one thousand, 3-inch x 4-inch PCBs down the line as “singles,” because of the time it takes to perform each of the assembly manufacturing steps.



To reduce manufacturing time, the manufacturing engineer will work with the PCB supplier to order the PCBs in an array form. A manufacturing panel array will make it possible for many PCBs to be processed together on a single manufacturing panel which will carry all the PCBs down the manufacturing line together. An array of PCBs

organized onto a panel in a 3-inch x 5-inch configuration could yield 15 completed PCBAs after a single pass through the assembly line, effectively reducing the manufacturing run time for the PCBA to 1/15 when compared to a single. This is a huge time savings to the manufacturing engineering stake holder who measures success or failure of process timing steps in seconds.



Besides a good overview of the PCB assembly process, what does a PCB designer need to do to create the best manufacturing panel array for the design? Surprisingly, very little. In fact, unless the design is going to be processed by the PCB designer's own company, don't do it. Assembly paneling is best determined by the assembly stakeholder, based upon their manufacturing requirements. If the PCB designer does not know where the PCB is destined to be built and knows nothing about the provider's equipment or capability, it is best to leave the design as a one-up and let the assembly provider do the rest to fit their process. The singulation method (sometimes referred to as excising or de-paneling) of the finished PCBA must be determined based upon the board outline shape. The process of singulation is accomplished using one of three common processes—V-scoring, tab-routing, and punching—each of which requires uniquely different panel design specifications.

Assembly paneling is best determined by the assembly stakeholder, based upon their manufacturing requirements.

You may be wondering, if PCB designers have very little to do with the creation of the manufacturing panel array, why do I need to worry about it? Well, the fact is regardless of the excising method used, the PCB assembly stakeholder will need space inside the board edge to perform the operation. Therefore, it is important for the PCB designer to understand the processes and requirements needed to create a manufacturable design. For example, often overlooked is the IPC recommendation to provide approximately .020 [0.51] clearance between the nominal PCB outline and all copper on the PCB to allow for successful assembly processing.

IPC-2221 & IPC-2222 provides some excellent guidelines for helping your EMS provider create manufacturable, cost effective panels from your design. Since the main goal of this guide is to help you have a basic understanding of the design process, below is an overview of common excising processes and what information you might need to consider when designing.

V-Scoring

V-Scoring is accomplished by the machining of shallow, linear cuts on both sides of PCB panel, each defining the edge of the rectangular PCB. The depth of the cuts penetrates approximately 1/3 into the PCB from each side, leaving approximately 1/3 of the PCB material left to constrain the PCB in the panel during the assembly operations. After assembly, the panel is moved to a “pizza cutter” type device which utilizes a sharp, round blade to cut the remaining web material in the v-score and break the PCB free.

V-Score Cut Cross Section

- ✓ Quick and efficient to produce.
- ✓ Best use of material; PCBs can be panelized edge-to-edge.
- ✗ May only be used on straight-edged PCBs.
- ✗ Broken web leaves an unsealed, lower-tolerance rough edge.
- ✗ Not suitable for very thick or thin PCBs due to constraints.
(Always check with the PCB supplier regarding capabilities).
- ✗ Not suitable for SMT parts which overhang the PCB outline.
(Some connectors are designed to overhang).

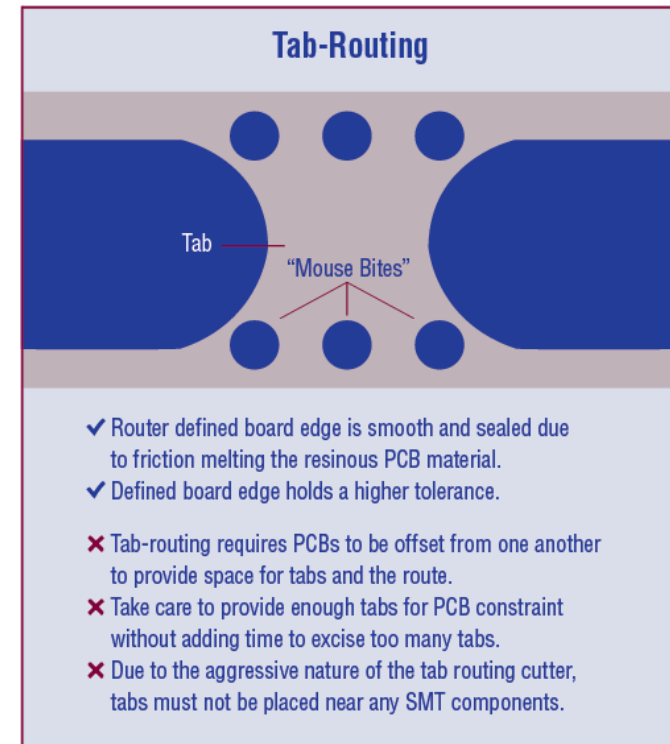
Tab-Routing

For PCB designs which cannot tolerate v-score, tab routing is an excellent option for the assembly stakeholder. Tab-routing requires a certain amount of space around the PCB outline to allow for a routing operation to remove all the material between the board edge and the panel. Without a web, as with v-scoring, the individual PCBs would simply drop out of the panel if it were not for a few keenly placed “tabs” which the panel designer strategically places around the PCB perimeter to “tack” and constrain the PCB within the panel. The tabs are formed by the high-speed routing tool exiting the route path for a few millimeters and then plunging back in to continue cutting the outline. Like the v-score webs, the tab-routed tabs remain in place throughout the assembly process. In the case of tab routing, the PCBAs are singulated using a pneumatic hook cutting-device, especially designed for removing tabs. The hook cutter enters from the bottom side of the PCB route and pulls downward on the tab, crushing the material away from the PCB edge. Depending on the design of the tab, this operation can leave a quite nasty burr on the board edge. Most tab route details will include the provision of several small, drilled holes added to the tab to further minimize the material in the tab and yield a smoother break. When these holes are added to the tab, the tabs are commonly referred to as “mouse bites.”

Punching

On very high volume PCBA runs, a punching method can be utilized to shear the PCB assemblies away from the panel. This process typically requires the use of non-glass and non-fibrous material such as the CEM family of laminates. There are very exacting design criteria

which must be considered to provide allowances for the punch/die equipment to perform properly. It is highly recommended to contact the PCB supplier if there is any possibility for the punch excising method to be used.



Like previously mentioned, while the designer does not have much involvement in the creation of the PCB array, it is important you understand what is involved so you can make sound design decisions. This way when the design is ready for production, you will avoid any manufacturing hiccups.

The best-case condition for wave soldering is when all the parts are mounted on the top side of the PCB.

Programming the Placement Machinery

Once the parts (including the PCB panels) are purchased, the automated assembly process can begin. The data required for this phase of the manufacturing process is taken from a few valuable sources. While the parts were being purchased, the manufacturing engineer was evaluating the bill of materials to get a general preview of the parts to be installed. For the manufacturing engineer, the BOM provides a limited view of the requirements. Along with the BOM output, the designer has hopefully provided an intelligent data format file for the design. With this information the manufacturing engineer can get a good look at the design intent and begin planning the order of manufacturing operations. Invaluable to the process is the provision of X,Y placement data output from the design database.

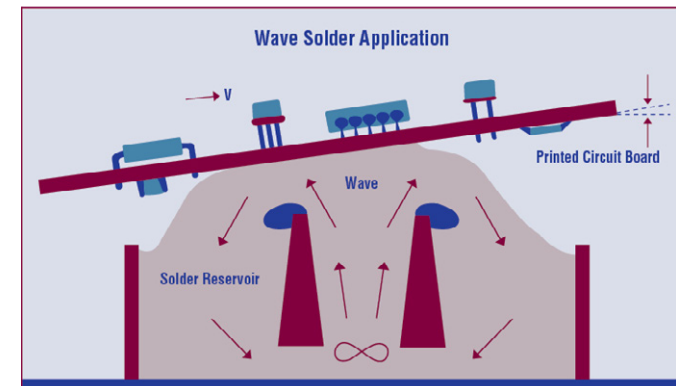
Sometimes referred to as a “pick & place” file, the data can be fed into process programming to help select the proper tape reel and define the nominal location and rotation for each SMT part which will be automatically soldered onto the board as required.

If there are SMT parts on both sides of the board, the placement file will indicate this and the placement parameters will be divided into two operations (the first pass and the second pass) to place and solder the SMT parts onto their respective sides.

In many cases, through-hole technology parts can be automatically assembled onto the PCB and run through the reflow process along with the SMT parts utilizing a newer, “paste-in-hole” process. These types of parts will need to be included in the X,Y placement file and will be specially handled by the manufacturing engineer.

All the remaining through-hole parts which are not to be run in the reflow oven process will be designated for secondary solder processing. This can either be done manually by a soldering technician or by two other common automated processes, wave soldering and selective soldering.

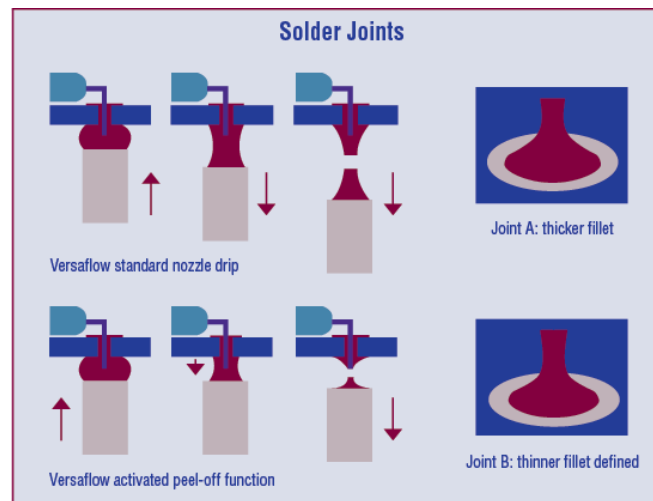
Wave soldering is widely utilized by the EMS provider to make solder joints on the side of the PCB in which the through-hole pins protrude. The best-case condition for wave soldering is when all the parts are mounted on the top side of the PCB. Only the through-hole pins needing solder and the secondary side of the PCB should meet the solder wave. There are cases in which SMT parts can be wave soldered too, but this special processing requires component bodies which can withstand the heat of the molten solder wave and they be specially glued onto the secondary side PCB surface prior to the operation.



When SMT exists on both sides of a mixed technology PCB design, it is far more common to process both sides of the PCB SMT passes in the reflow oven. Then follow up with a selective solder operation for the remaining through-hole parts on the assembly.

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Selective solder machinery can make very accurate solder joints on through-hole component pins by positioning a small fountain of solder underneath the selected pin and automatically raising the fountain cup enough to make the solder joint. The process is highly accurate, but is not considered “speedy” due to the nature of the single-solder fountain head.



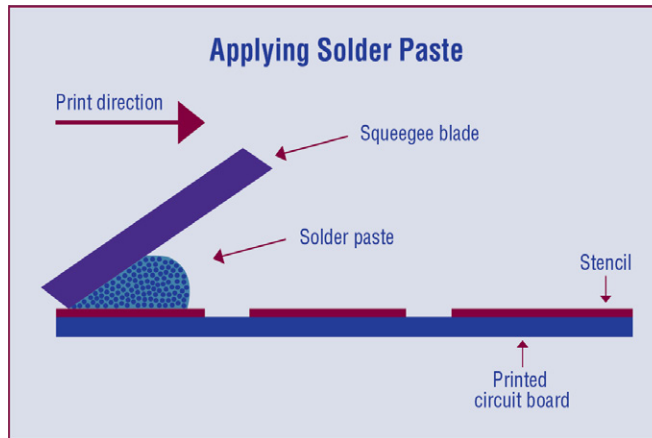
Many important decisions must be made regarding solder processing before a board ever begins to roll down the assembly line. It is important for the PCB design engineer to understand that even though the EMS provider has many options to address the manufacturing challenges which cascade onto the planning department tables every day, the goal of the PCB design engineer should be to communicate with the manufacturing engineering stakeholder. Seek out design solutions to reduce these multiple process requirements as much as possible; that's just good DFM.

Applying the Solder Paste

All the SMT components which are to be placed upon the PCB during the pick & place operation already have etched copper lands ready to contact the contacts of the parts. The manufacturing material and process to make this connection is called soldering and is accomplished using several methods.

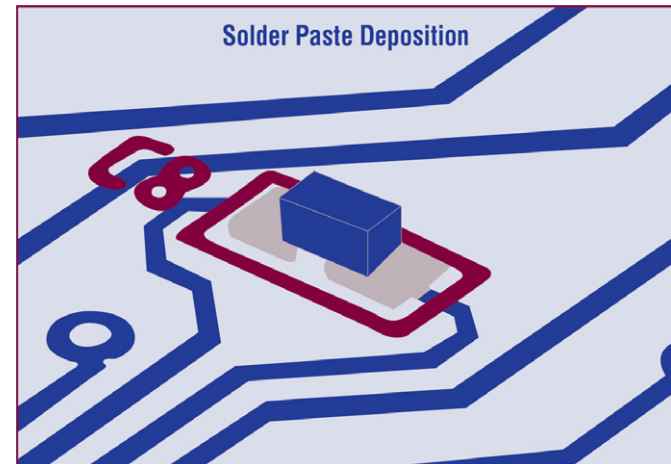
There is an automated process for applying just the right amount of solder paste to each pin and land pair. The solder paste deposition process utilizes a unique machine to position the PCB panel, so it can meet a metal “stencil” with specially formed openings for the solder paste material to squeeze through and become deposited onto the land. Where does this stencil come from? After the PCB designer has sent the PCB manufacturing data package to the EMS provider, the manufacturing engineer looks for a pastemask or stencil artwork file in the package. Like all the files in the design, the stencil file is provided one-up. At this point, it is the responsibility of the manufacturing engineer to push this file to a stencil manufacturer who will cut the stencil based upon the artwork file and the array specification drawing provided by the EMS provider.

When ready, the panel is loaded into the stencil machine and aligned with the stencil using the panel fiducials added by the supplier. The stencil has electro-formed markings accurately positioned to align with the fiducial markings on the panel. The alignment process is optically-based and very accurate. Once the PCB panel has been screened with solder paste the assembly process must move quickly.



The solder paste deposition is inspected to look for a good “release” of the stencil, forming just the right amount of solder deposition onto the land. The solder paste holds its shape after stencil release because it is composed of tiny spheres of solder suspended in a tacky flux resin. This sticky solder paste serves as an excellent temporary “adhesive” for attaching components to the PCB before they will be permanently soldered.

During soldering, the flux resin will vaporize and serve to provide an inert local environment condition for the solder to bond to the land and the component pin cleanly.



Automated Placement

After solder paste is applied, the panel moves onto the placement line. The panel is designed to include rails, which not only provide stability to the panel structure, but support the panel on the conveyer as the panel is moved into position for automated placement. The pick-and-place machinery optically calculates the exact position and rotation of the panel, again by means of optical sensors which recognize the fiducial markings added to the panel. Since the coordinate starting point of the panel is known by the pick and place machine via the placement file provided by the PCB designer, the machine can populate all the components onto the panel with lightning speed. A placement head races to a reel to pick up a specific part using a vacuum nozzle, the orientation of the part on the nozzle is measured, and then while moving toward the component's X,Y location the nozzle is rotated to match the exact angle of the footprint on the PCB panel image so the part is accurately placed.

Moving Through the Reflow Oven

Once all the parts are placed onto the side under assembly, the PCB panel moves along the conveyor into the assembly reflow oven to heat the assembly, melt the solder, and form perfect solder joints. (Ref: IPC-A-610.)

A few variables must come together well for solder joints to be in spec.

- First, the footprint land geometry must be designed properly with enough toe and heel and side extension to allow for a perfect solder fillet. (Ref: IPC-7351)
- Second, the optimal amount of solder paste must have been applied to the land by accurately calculating the stencil opening in relation to the stencil thickness and the type of solder being used on the PCB.
- Third, the oven's thermal profile (or heat zones) must be adjusted just right so the PCB and components receive the proper thermal ramp, soak, and cooling times, to allow the solder to flow and solidify properly.

Second Op Assembly Processing

As mentioned, parts which are not suitable for the reflow oven must be processed using different manufacturing practices. It is usually up to the manufacturing engineer to determine how these remaining components will be soldered. The PCB assembly drawing the designer provides should specify the components be “soldered” without being specific with regards to how. This is intended to allow manufacturing flexibility for the owner of the assembly process (more on that soon).

There are through-hole parts which must be addressed specially with alternative soldering processes such as wave and selective soldering, but there are many other types of assembly actions required on the PCBA after all the parts are soldered. It is important for these second-op conditions to be carefully considered by the PCB designer during the layout phase, hopefully in collaboration with the manufacturing engineering stakeholder. However, since the design has been released and all the parts have been procured, it is time for the manufacturing engineer to have the latitude to adjust any processing based upon the physical parts in hand. For instance, a tall capacitor may be getting knocked around during a cable routing operation. The manufacturing engineer will need flexibility to add a constraint material to the capacitor, like RTV, to support the part and protect the solder joints prior to cable routing to address this unforeseen issue. This is only one of many things which will eventually be addressed in the PCBA drawing specification. Ultimately, it is up to the design and engineering stakeholders to define the performance requirements of the product. How the manufacturer gets there is ideally left up to them. Here are some examples of other items which can be addressed:

- Addition of trace cuts or adding jumper wires
- Adding any lap soldered wire harnessing
- Adding potting material around moisture sensitive circuits
- Adding conformal coating over the PCBA or in selective areas
- Adding special marking and labels for identification
- Adding mechanical hardware with any thread torquing requirements

Assembly Test

Once all the assembly operations and processes have been run, verification must take place in order for the PCB assembly to be validated for performance. This is the point where all of the front-end investment of time and expense to add test points and create fixtures and software mentioned in chapter 6 is going to pay off. If everything has gone according to plan, the PCBAs are taken from the line and placed into the assembly test fixture. There is a program which will be run in order to check for continuity between parts to ensure all of the soldering and placement has gone smoothly. The tests are designed to run quickly because cycle time is valuable. There are checks for functionality which will supply power in order to light LEDs and run displays. The test engineers have collaborated with the PCB design engineer to make certain every function of the PCBA will be tested and will perform within specifications.

What if a problem is found? Actually, this is good news! This is the purpose of the assembly test process. If a problem is found such as a mis-located part or even an incorrect part, the board can be set aside for rework. After rework, the board will have to run through the entire assembly test process again to ensure complete conformance.

Final Inspection (IPC-A-610)

At last, the PCBA is ready for final inspection. There are a few assembly notes which may be deemed necessary on an assembly drawing. Perhaps marking requirement notes, hardware torque tightening specs, maybe a dot of RTV here or a tie wrap over there. None are as important or carry so much weight and responsibility for measuring design quality as IPC-A-610. Adding a simple note: “Acceptance criteria per IPC-A-610,” says all the right things to your final inspection department. The pictorial, easy to read specification covers basic conditions of every basic process which your PCBA will have been exposed to during its journey through the assembly shop. The point has been made throughout this book—from Ian’s early experiences entering data into a layout without any manufacturing knowledge, to the introduction to the many stakeholders of the PCBA design and manufacturing process—that the success of an entire project is based upon getting electrons to flow through an automatically assembled circuit with repetitive success. In summary, every topic and character description in this book illustrates a relative interconnectivity between stakeholder responsibilities interconnection to the design manufacturing and assembly process.

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By the time a PCBA has reached the point of final inspection, many hours of time and material have been invested. There have been literally thousands of things which could have gone wrong. In fact, many things probably did. However, because of the incredible inspection points which are implemented throughout the many processes, the problems were identified and corrected allowing material to pass through correctly. IPC-A-610 and the many other specifications which are utilized to compare manufactured hardware with conforming or non-conforming criteria are invaluable guidelines for final assembly test technicians to use to measure how each stakeholder has done their job. Once all the solder joints are inspected, once all the parts are inspected, once the PCBA is run through its required burn in testing and has passed, the manufacturing process is complete and the PCBA is ready to be shipped out to perform its purpose in the consumer or industrial world. It is the hope of all the contributors of this book that its message of collaboration, communication, and understanding will serve the designer well as they assume an influential role as the hub of the entire design and manufacturing process for the PCBA.

Conclusion

Within the PCB assembly process or any PCB related process, literally tens of thousands of things can go wrong. That a PCBA can be brought together with hundreds of other parts to be exposed to dozens of processes and come off the final inspection line with “PASS” stamped upon its board surface seems a jaw dropping miracle. However, to those stakeholders who take the time to reach out – to communicate, to collaborate – the result is not miraculous. It makes perfect sense; it is a matter of perspective. The fully-engaged stakeholder knows the processes inside-and-out and has learned from each assembly, each cycle, and has made the required adjustments. So must the PCB design engineer. If there is anything to learn from the disciplines of the manufacturing and assembly floors it is that a process of checks and verification must be in place at every step. Data and documentation created by the PCB design engineer on the front-end must be clean. Garbage in equals garbage out, as they say. We would be amiss not to once again encourage the PCB design engineer to contact a local EMS provider to schedule a plant tour to see for themselves the disciplines, the order, the cleanliness by which PCBA's are produced. Get out and observe the causes of manufacturing success and failure. Learn from your assembly manufacturing brethren to incorporate the tangible causes of success into your own PCB design process.

Pro Tips

- ☐ It is very important that a complete package of data is supplied to the assembly stakeholder including a BOM, neutral database file, XY placement file, solder paste stencil artwork file and test point location file.
- ☐ The sooner the component information can be captured and sent to the purchasing agent, the better.
- ☐ The exported BOM must list all the electronic and mechanical parts used in the assembly, including the bare PCB, all components, and even mechanical hardware, adhesives, coatings, and wire.
- ☐ As with the PCB provide the assembly stakeholder with a neutral database such as ODB++ or IPC-2581.
- ☐ Make sure the X,Y placement file specifies a reference designator side of placement, X,Y location, and angle of orientation for each part.
- ☐ If the assembly will be implementing DFT, include a test point report file which include net names, side of access X,Y location and test point names if applicable.
- ☐ Prior to release, always pull BOM information from the source schematic.
- ☐ Consider that the PCB assembly drawing is less of a how-to document and more of an inspection document.
- ☐ PCB Assembly drawing should include a pictorial view, component outlines, reference designators, any special details and notes.
- ☐ Even if you are not the one who will be doing the work, consider how your design will be panelized for volume assembly.
- ☐ Consider the importance of leaving space $\geq .020$ [0.51] clearance between the PCB edge and any copper to allow for singulation of the PCBA from the panel using v-score or tab-route options.
- ☐ Consider the importance of biasing thru-hole components to the top side of the assembly so the wave solder operation will have easy access to component pins.
- ☐ Consider it part of your design job to communicate often with the assembly supplier stakeholder.
- ☐ Provide 1:1 ratio openings on stencil artwork and allow the stencil supplier to coordinate compensation and adjustment with the assembly manufacturing engineer.
- ☐ Think about implementing DFT at the layout stage. It's probably too late to begin thinking about it at the PCB documentation stage.
- ☐ Leverage the power of IPC-A-610 to define the acceptance criteria for your PCBA. It has stood the test of time as a comprehensive conformance guideline.

Chapter 42

The Future



Ian pushed the button on the side of his VR goggles. “Shutting down” the screen read. Ian reached back to loosen the straps and pulled the cowl from his face.

Ian waited a moment for his eyes to adjust. His experience using Old Bob’s VR glasses to connect with project stakeholders seemed like a three-day trip. He was tired and his temples were aching.

Ian had spent the last 24 hours communicating with the stakeholders of the project. The short time he spent listening and learning from Old Bob and the project stakeholders was very much like immersion training. Ian now fully understood his role and could carve out a process he could implement in the future. This not only helped get his part of current and future projects completed on time, but also gave him the confidence knowing it was done correctly. Ian could not be happier.

Ian reached for the old phone on his desk and dialed 42. He wanted to speak to Old Bob to thank him for all his help. Ian heard a dial tone and a couple of beeps on the other end. Just then, a scratchy voice recording responded,

“Thank you for calling RoHaws EMS. Bob Gridmaster is out of the office enjoying a well-deserved vacation on Planet X. Thank you and have a nice day.”

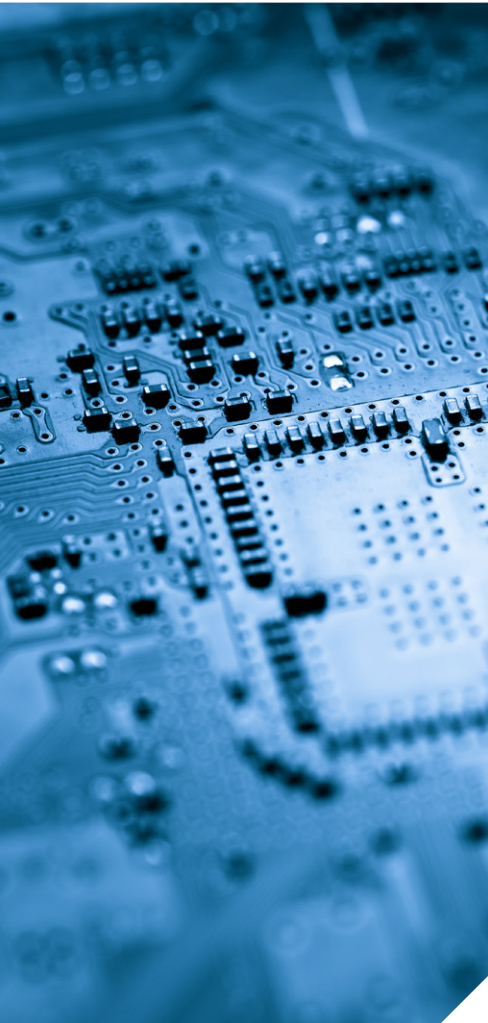
Ian then hung up the receiver, wiped his brow with a towel, and began designing his next project.

Preparing for the Next Electronic Generation

Ian’s story is an all too common occurrence amongst new engineers. However, once these engineers become armed with knowledge and couple it with the support of additional project stakeholders, they can rest-easy knowing their design process has started off on the right track. The goal of this book is to help empower engineers with the knowledge needed to understand design fundamentals, effectively leverage today’s technology, and learn from the mistakes others have made in the past.

While the advent of automation and the latest software capabilities have made it much easier for even the most inexperienced users to “complete” full designs, like our protagonist Ian quickly found out, lack of design fundamentals and collaboration can lead to major issues later and make it almost impossible to leverage the technology available to its fullest potential. We forget tools are just tools; they don’t always solve the problems a designer can run into during the design process. It’s the person operating those tools who does this. Knowing what and why your CAD program does what it does, coupled with expert knowledge of PCB design, will (usually) make for a more streamlined and pleasant experience.

The future is driven by the constant evolution of technology. No matter where you are in your career, this will always continue. To be remain successful, designers are going to have to find ways to quickly adapt. Ultimately, it is about adequately preparing for the next electronic generation.



With emerging technologies such as 3D printing, artificial intelligence, and machine learning becoming synonymous with daily life, its impact on the design process is all but inevitable. The emergence of 3D printers from companies such as Nano Dimension, Ltd., Voxel8, and Siemens, has made the idea of 3D printed circuits a reality. “From a micro-perspective, I firmly believe an engineer of the future is going to be sitting at his/her desk and is going to click ‘file > print’ and over in the corner there is going to be a 3D printed circuit board printer, just knocking out a prototype board,” said Manny Marciano, CEO of EMA Design Automation.

As we continue to look towards the future, we can see ECAD and MCAD are slowly beginning to become synonymous with one another. This convergence is causing the emergence of a new discipline called Mechatronics, and its adaptation is going to change how engineers of the future will work. We are heading in this direction already. The desktop workflow of the future is going to be a mechatronics solution where many of the individual disciplines we know today will be absorbed into one consolidated engineering profession. Knowing how to properly design a printed circuit board will provide engineers with the foundation they need to be successful.

The Role of the Electrical Engineer is Changing

The process of PCB design is evolving and with that, so is the role of the Electrical Engineer. What was once a highly segmented process—a separate person in charge of libraries, schematics, PCB layout, DFM, etc.—has now converged into a single job role. This new role, the ‘PCB Design Engineer’ or whatever other title it might be called in the future, requires one to not only understand every aspect of the PCB design process, but the tools which will ultimately help accomplish these myriad of tasks on-time and on-budget. Having a complete understanding of the design processes will ensure utilization of these evolving technologies to their fullest potential.

In addition, we are also seeing the convergence of the role of both the Electrical Engineer and the Mechanical Engineer. Merging both electrical and mechanical knowledge is slowly becoming essential to creating a proper design at the Mechatronics level. Engineers must adapt and become the reference point for the other specializations.

Few people will be doing the job of many, basing their design workflow on automation and resources available on an industry-wide basis. Since the electronics industry is already known for having a competitive landscape, designers will have to constantly review trends and evolve with them. Those armed with a fundamental understanding of design and manufacturing process will set themselves apart from their peers.



Using this Book as a Resource

Ultimately, we wanted this book to be another resource in your toolbox. At the end of each chapter is a checklist highlighting the key points from each chapter. You can print these and use them as quick guides to reference as you work. However you choose to utilize the information within this guide, we are confident the information included will help you to be successful while on your PCB design journey.

So Long and Thanks for all the Fish

No matter how you cut it, technology and automation are a requirement today. However, since the tools don't have the capability to understand what's in your head (yet) it is up to you, the PCB design engineer, to define this. While it is important to embrace technology and automation, it is essential to understand your design parameters to move forward. This guide will help you do this.

As the role of the designer evolves into the hub of the entire design and manufacturing process for the PCBA, it is the hope of all those who contributed to this guide, that its message and content will serve as a valuable resource.

Ultimately, everything boils down to having an open mind, so you can quickly adapt as technology changes and learn how to apply lessons from the past. Failure to do so could not only prevent you from completing your design successfully, but it can also keep you from reaching your full potential.

Simply put, all you need to be successful in this quickly-evolving industry are this guide, a towel, and an open mind.

The Hitchiker's Guide to PCB Design by EMA Design Automation
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www.ema-eda.com

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